



## 30V, 1A CC&CV Synchronous Buck Converter

### FEATURES

- Up to 97% Efficiency
- Input Voltage Range: 4.5V to 36V
- Continuous Output Current: 1A
- CCM Switching Frequency: 150KHz
- Reference Voltage: 0.9V  $\pm$ 2% @25°C
- Maximum Duty Cycle: 98%
- Integrated MOSFETs: 250mΩ and 140mΩ
- Peak current mode control
- Over Current Protection
- Input over voltage protection
- Output over voltage protection
- Short Protection
- Pulse skip mode at light load to improve light load efficiency
- Internal Soft Startup
- Thermal Shutdown Protection

### APPLICATIONS

- USB car charger
- Portable charging device
- General purpose DC-DC conversion

### DESCRIPTIONS

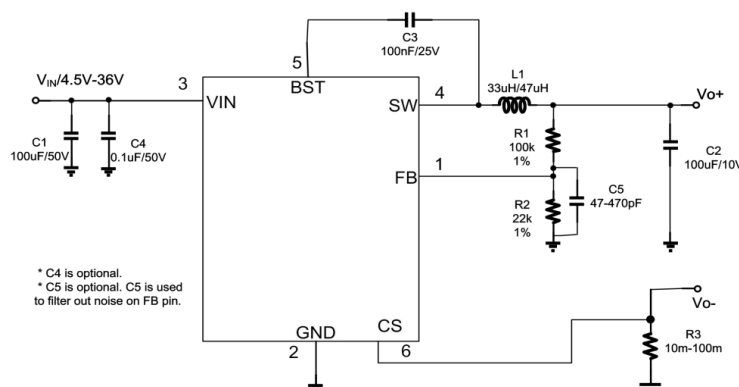
DP31231C/B is a monolithic 36V, 1A step-down switching regulator. DP31231C/B integrates a 36V 250mΩ high side and a 36V, 140mΩ low side MOSFETs to provide 1A continuous load current over a 4.5V to 36V wide operating input voltage with 33V input over voltage protection. Peak current mode control provides fast transient responses and cycle-by-cycle current limiting. DP31231C/B has configurable line drop compensation, configurable charging current limit. CC/CV mode control provides a smooth transition between constant current charging and constant voltage charging stages. Built-in soft-start prevents inrush current at power-up.

The DP31231C/B requires a minimal number of readily available, external components and is available in a small package.

### ORDERING INFORMATION

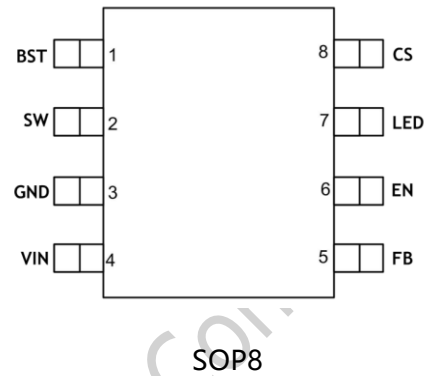
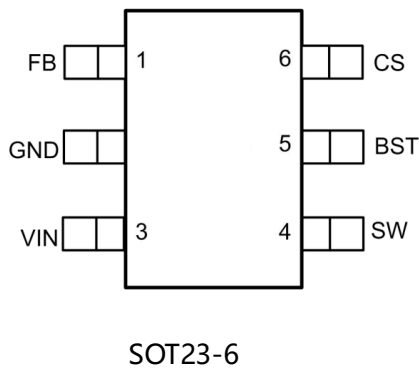
Part Number	Description
SOT23-6	Pb free in T&R, 3000 Pcs/Reel
SOP8	Pb free in T&R, 4000 Pcs/Reel

### TYPICAL APPLICATION CIRCUIT



## PRODUCT DESCRIPTION

### ➤ Pin Arrangement



### ➤ Pin Configuration

SOT23-6	SOP8	Pin Name	Description
5	1	BST	Supply input for the high-side NFET gate drive circuit. Connect a 0.1μF capacitor between VBST and SW pins.
2	3	GND	Ground Pin
1	5	FB	Feedback pin for the internal control loop. Connect this pin to an external feedback divider.
6	8	CS	<p>Current sense input. Connect a 10mΩ to 100mΩ resistor between this pin and GND to program current limit. CS pin is also used to set the work mode as following:            Work Mode 1: When CS pin is connected to GND through a current sense resistor, CC loop will be enabled. The current limit will be set by the sensing resistor. R1 in Fig. 1 can also be used to program line drop compensation.</p> <p>Work Mode 2: When CS pin is connected to GND, The output voltage is set with a resistor divider from the output node to the FB pin. 1% resistance accuracy of this resistor divider is preferred. The output voltage value is set as equation 1 below (R1 is the upper resistor, R2 is the lower resistor)</p>
3	4	VIN	Power supply voltage input.

4	2	SW	Switch pin connected to the internal FET switches and inductor terminal. Connect the inductor of the output filter to this pin.
-	6	EN	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator; low to turn it off. EN pin is pulled to VIN internally by a larger resistor. EN threshold is set to 1.1V without hysteresis.
-	7	LED	LED input. Connect the negative terminal of a LED to indicate output status.

### ➤ Marking Information



DP31231 for product name:

YYY refers to the following table description, represents different packaging and special functions

XXXX The first X represents the last year, 2020 is 0; The second X represents the month, in A-L 12 letters; The third and fourth X on behalf of the date, 01-31 said;

Marking	Model	Description
31231B	DP31231BST	DP31231BST Buck, 4.5V~36V, 1A, 150KHZ, VFB 0.9V, <b>DCM</b> , SOT23-6
31231C	DP31231CSO	DP31231CSO Buck, 4.5V~36V, 1A, 150KHZ, VFB 0.9V, <b>DCM</b> , SOP8

## ➤ Absolute Maximum Ratings

PARAMETER	Min	Max	Unit
VIN Voltage	-0.3	36	V
EN Voltage	-0.3	6	V
SW Voltage(DC)	-0.3	36	V
SW Voltage(AC less than 10ns while Switching)	-1	36	V
Vcs Voltage	-0.3	6	V
FB Voltage	-0.3	6	V
BS Voltage(vs SW)	-0.3	6	V
Operating junction temperature,TJ	-40	150	°C
Storage temperature, Tstg	-65	150	°C
Lead Temperature (Soldering, 10sec.)	-	260	°C

Note:(1)Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability. Over operating temperature range (unless otherwise noted)(1)  
 (2) All voltage values are with respect to network ground terminal

## ➤ Recommended Operating Conditions

PARAMETER	Min	Max	Unit
VIN Voltage(VIN)	6.5	30	V
Output current(IOUT)	0	1	A
TJ	-40	125	°C

Note : (1)All limits specified at room temperature (TA = 25°C) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL)

## ➤ ESD Ratings

PARAMETER	Description	Value	Unit
HBM	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
CDM	Charged-device model (CDM), per JEDEC specification JESD22-	±500	V

Note : (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control

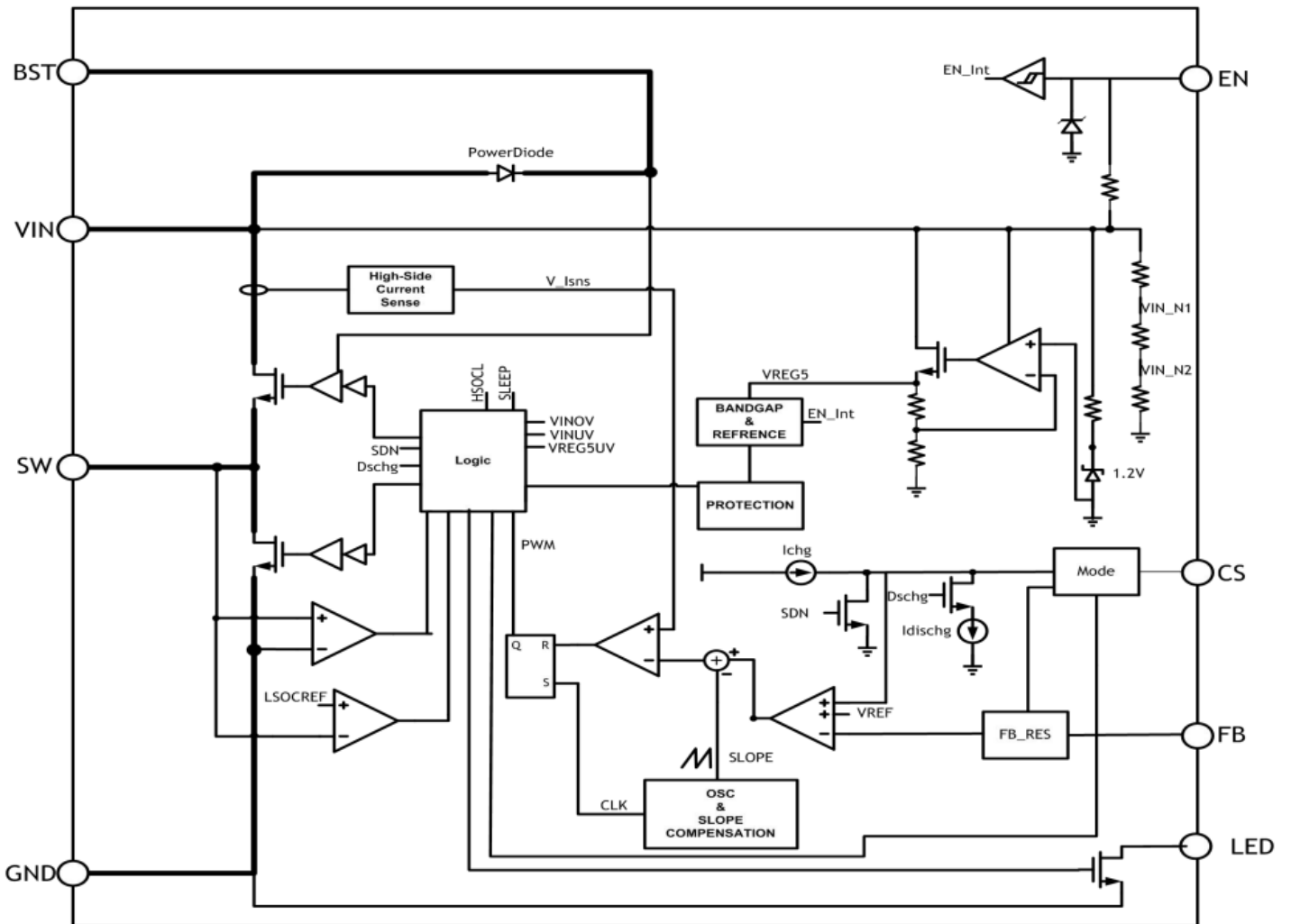
## ➤ Thermal Information

THERMAL METRIC	Description	SOP8	SOT23-6	Unit
R $\theta$ JA	Junction-to-ambient thermal resistance(1)(2)	48.7	121.6	°C/W
R $\theta$ JC(top)	Junction-to-case (top) thermal resistance	52.4	69.1	°C/W
$\psi$ JB	Junction-to-board characterization parameter	25.2	46	°C/W
R $\theta$ JB	Junction-to-board(Bottom) thermal resistance	25.5	45.5	°C/W
$\psi$ JT	Junction-to-top characterization parameter	8.4	22.3	°C/W

Note (1): The package thermal impedance is calculated in accordance to JESD 51-7.

Note (2): Thermal Resistances were simulated on a 4-layer, JEDEC board

**BLOCK DIAGRAM**



Developer

## ELECTRICAL CHARACTERISTICS

(Typical at  $V_{IN}=12V, T_J=25^{\circ}C$ , unless otherwise noted.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Shutdown Current	ISHDN	$V_{EN}=0V$		3		$\mu A$
VIN UVLO Rising Threshold	VUVLO(R)	$V_{IN}$ Rsing			4.4	V
VIN UVLO Falling Threshold	VUVLO(F)	$V_{IN}$ Falling		4.3		V
VIN UVLO Hysteresis	VUVLO(HYS)			0.3		V
VIN OVP Rising Threshold	VOVP(R)	$V_{IN}$ Rsing		33		V
FB Voltage	VFB	$T_J=25^{\circ}C$	0.882	0.9	0.918	V
FB Leakage Current	I <sub>FB(LKG)</sub>	$T_J=25^{\circ}C$	-100	0	100	nA
Switching Frequency	F <sub>sw</sub>	Operation CCM		150		KHZ
Max duty cycle	D <sub>max</sub>				98	%
Mini on Pulse Width	T <sub>ON(MIN)</sub>			100		ns
High-Side Switch Current Limit	I <sub>HS(OC)</sub>	$V_{IN}=12V, V_{FB}=90\%$		3.5		A
Low-Side Switch Current Limit	I <sub>LS(OC)</sub>	$V_{IN}=12V, V_{FB}=90\%$		1.2		A
High-Side MOS ON-Resistance	R <sub>DS(on)(HS)</sub>	I <sub>sw</sub> =100mA		250		m $\Omega$
Low-Side MOS ON-Resistance	R <sub>DS(on)(LS)</sub>	I <sub>sw</sub> =100mA		140		m $\Omega$
Output Over Voltage Protection	V <sub>out_ovp</sub>			1.1*VFB		V
Over-Temperature Protection	T <sub>SD</sub>			155		$^{\circ}C$
Over-Temperature Protection hysteresis	$\Delta T_{SD}$			15		$^{\circ}C$

## TYPICAL CHARACTERISTICS

Test Condition: TA = 25°C, VIN=12V, Vout=5V, unless otherwise noted.

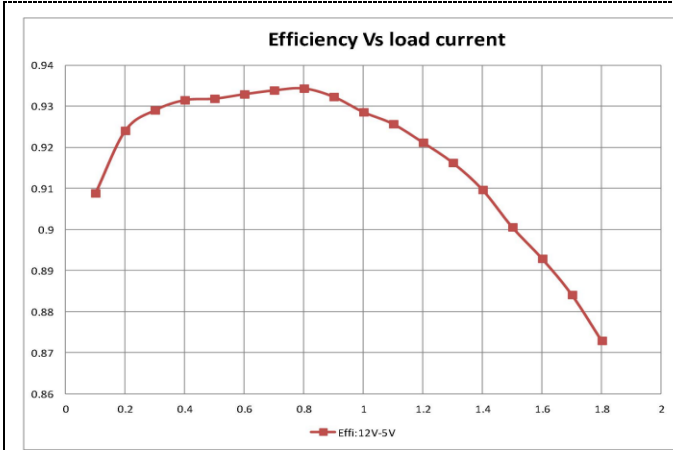


Figure1 12V to 5V Output Efficiency

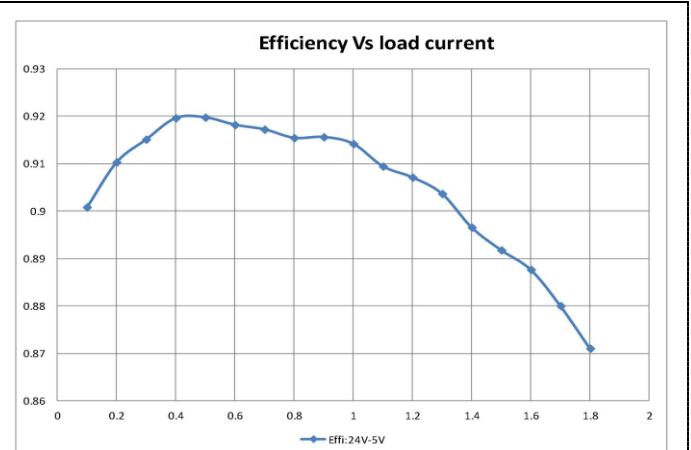


Figure2 24V to 5V Output Efficiency

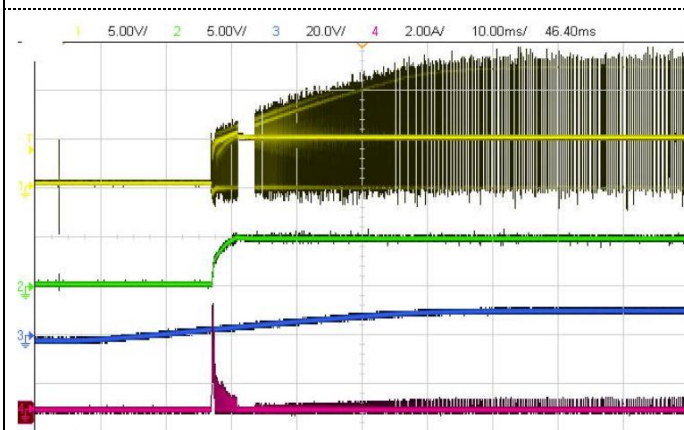


Figure3 Startup waveform, Iout = 0A

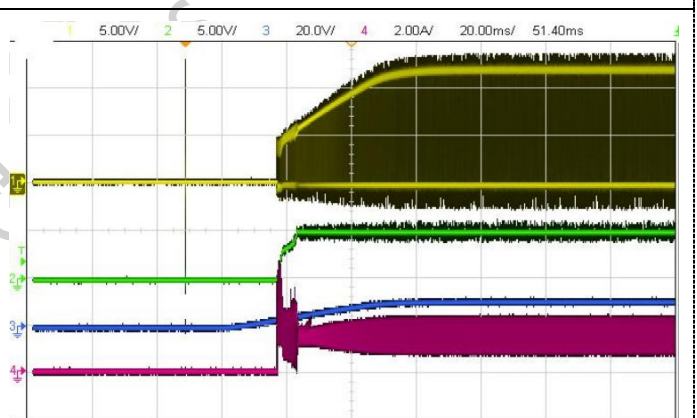


Figure4 Startup waveform, Iout = 1A

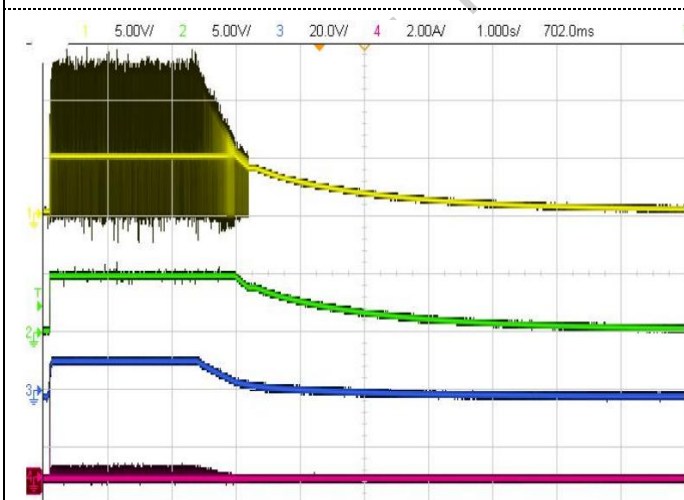


Figure5 Shutdown waveform, Iout = 0A

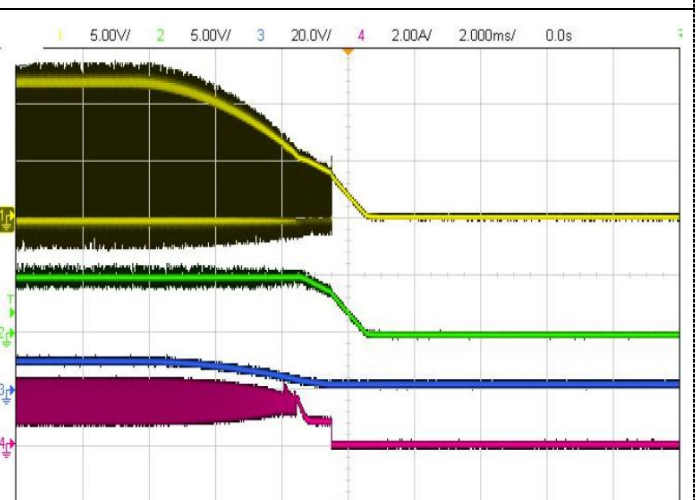
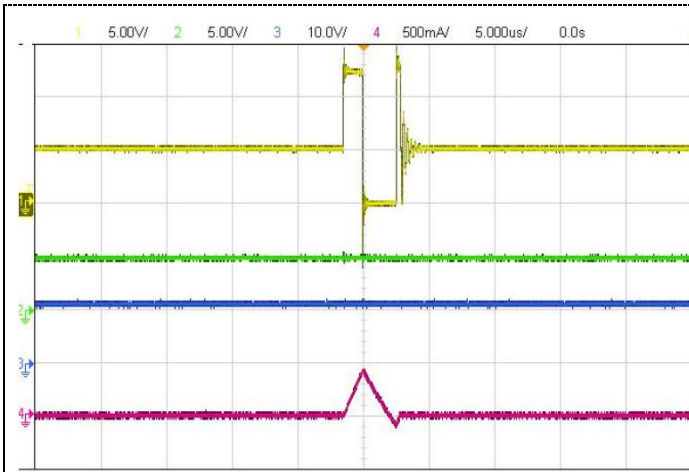
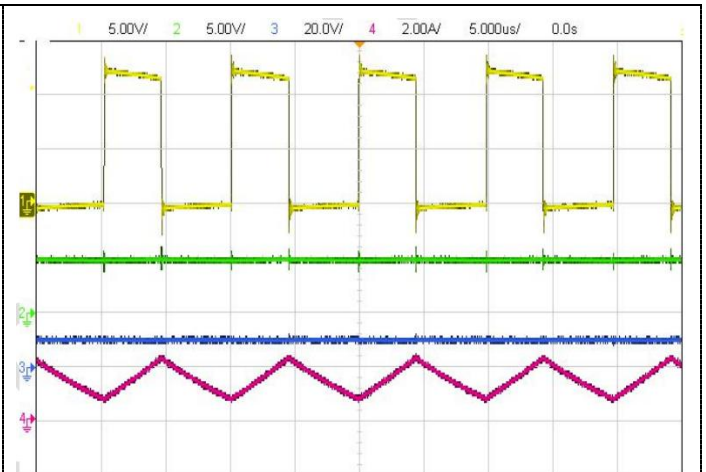


Figure6 Shutdown waveform, Iout = 1A



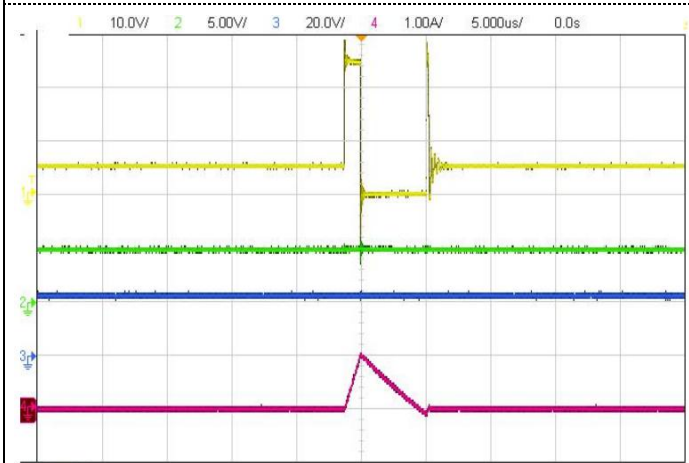
VIN=12V Vout=5V Iout=0A

Figure7 Steady state waveform



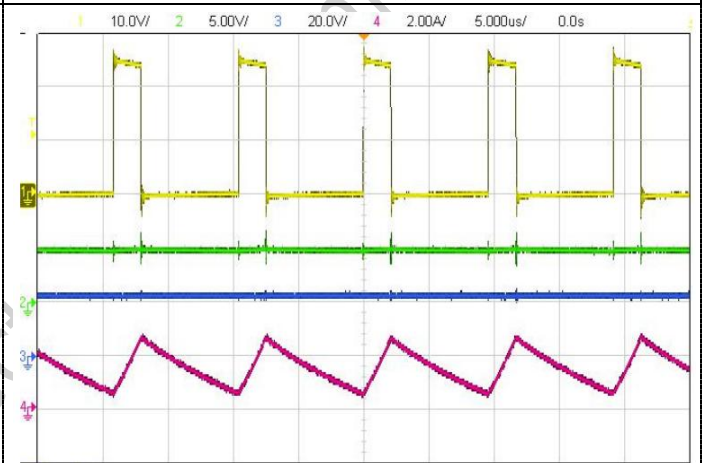
VIN=12V Vout=5V Iout=1A

Figure8 Steady state waveform



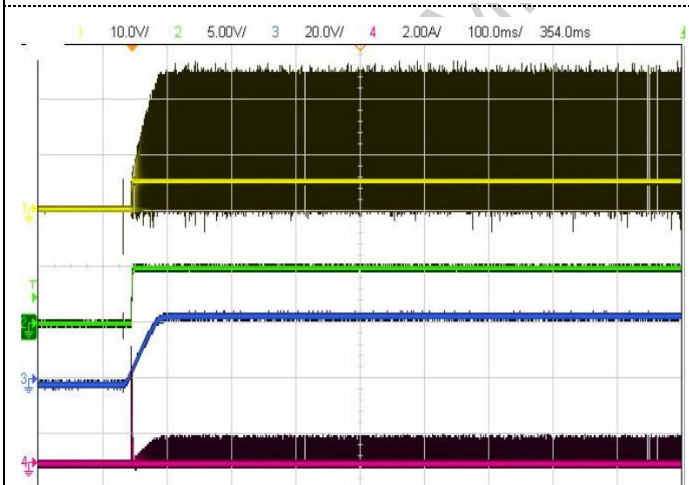
VIN=24V Vout=5V Iout=0A

Figure9 Steady state waveform



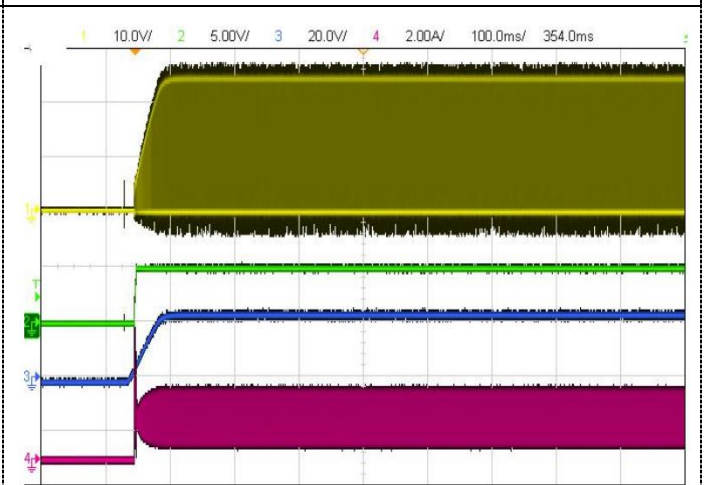
VIN=24V Vout=5V Iout=1A

Figure10 Steady state waveform



VIN=24V Vout=5V Iout=0A

Figure11 Startup waveform



VIN=24V Vout=5V Iout=1A

Figure12 Startup waveform

## FUNCTIONS DESCRIPTION

### ● Feature Description

DP31231C/B employs a fixed 150 kHz frequency peak current mode control. The output voltage is sensed by an external feedback resistor string on FB pin and fed to an internal error amplifier. The output of error amplifier will compare with high side current sense signal by an internal PWM comparator. When the second signal is higher than the first one, the PWM comparator will generate a turn-off signal to turn off high side switch. The output voltage of error amplifier will increase or decrease proportionally with the output load current. DP31231C/B has a cycle-by-cycle peak current limit feature inside to help maintain load current in a safe region.

### ● Thermal Shutdown

The internal thermal-shutdown circuitry forces the device to stop switching if the junction temperature exceeds 155 °C typically. Once the junction temperature falls below the falling threshold, the device returns to normal operation automatically.

### ● Startup AND Shutdown

The If both VIN and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries. Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The comp voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

### ● UNDER-VOLTAGE LOCKOUT (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. UVLO

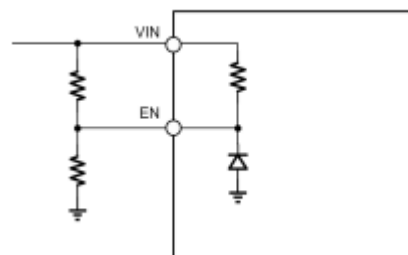
protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. When the voltage is higher than UVLO threshold voltage, the device is enabled again.

### ● INPUT Over Voltage Protection(OVP)

The DP31231C/B Integrates input over voltage protection. The OVP circuitry detects over voltage condition by monitoring the input voltage. When input voltage rises above the OVP threshold, the OVP comparator turns high and both HS-FET and LS-FET are turned off. Once VIN drops below OVP falling threshold, the IC starts switching again. This function can ensure the reliability when the input voltage is unstable with over voltage spike.

### ● Setting Enable Threshold

When the voltage at EN pin exceeds the threshold, DP31231C/B begins to work. When keeping EN low (below threshold), DP31231C/B stops working. The quiescent current of DP31231C/B is very low to maintain a good shut down operation for system. DP31231C/B has an internal pull up resistor to make sure IC work when EN pin is float. If an application requires to control EN pin, use open drain or open collector output logic circuit to interface with it. When system needs a higher VIN UVLO threshold, the EN pin can be configured as shown in below



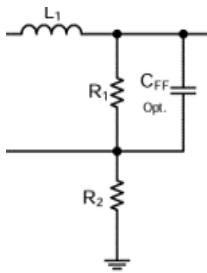
## APPLICATION INFORMATION

The output stage of synchronous buck converter is mainly composed of inductor and capacitors. By switching the internally integrated power MOSFET, the energy is stored and transferred to the load, and the second-order LC filter is formed to smooth the switching node voltage so that the stable output DC voltage is obtained.

### ● Setting Output Voltage

The output voltage is set by FB voltage, which is divided by resistor (R1 & R2) from output node to Ground. That resistor with 1% or higher accuracy is preferred. The output voltage value is set by equation as below.

$$V_{OUT} = V_{FB} \times ((R1 + R2)/R2)$$



Vref is the internal reference voltage of DP31231C/B, 0.9V.

### ● Inductor selection

An inductor is required to supply constant current to the load while being driven by the switched input voltage. The common value of the inductance is between 1uH to 22uH. A larger value inductor will result in less current ripple and lower output voltage ripple. However, the larger value inductor will have larger physical size, higher DC resistance, and/or lower saturation current. A good rule to calculate the inductance is to allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum load current. At the same time, it is needed to make sure that the peak inductor current is below

the inductor saturation current.

The inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_s \times \Delta I_L} \left( 1 - \frac{V_{OUT}}{V_{IN}} \right)$$

Where VOUT is the output voltage, VIN is the input voltage, fs is the switching frequency, and ΔL is the peak-to-peak inductor ripple current.

The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

The choice of which style inductor to use mainly depends on the price vs. size requirements and any EMI constraints.

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency

### ● Input capacitors selection

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the converter. It is recommend to use low ESR capacitors to optimize the performance. Ceramic capacitor is preferred, but tantalum or low-ESR electrolytic capacitors may also meet the requirements. It is better to choose X5R or X7R dielectrics when using ceramic capacitors.

Since the input capacitor (CIN) absorbs the input switching current, a good ripple current rating is required for the capacitor. The RMS current in the input capacitor can be estimated by:

$$I_{CIN} = I_{load} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left( 1 - \frac{V_{OUT}}{V_{IN}} \right)}$$

The worst-case condition occurs at VIN = 2×VOUT, where:

$$I_{CIN} = \frac{I_{load}}{2}$$

For simplification, choose the input capacitor whose RMS current rating is greater than half of the



maximum load current. When electrolytic or tantalum capacitors are used, a small, high quality ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible. When ceramic capacitors are used, make sure that they have enough capacitance to maintain voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{load}}{f_s \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

C<sub>IN</sub> is the input capacitance.

### ● Output capacitors selection

The output capacitor (C<sub>OUT</sub>) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_s \times C_{OUT}}\right)$$

Where L is the inductor value, R<sub>ESR</sub> is the equivalent series resistance (ESR) value of the output capacitor and C<sub>OUT</sub> is the output capacitance value. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly determined by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_s^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also

affect the stability of the regulation system. The DP31231C/B can be optimized for a wide range of capacitance and ESR values.

### ● Feed-Forward Capacitor Selector(CFF)

DP31231C/B has internal loop compensation, so adding CFF is optional. Specifically, consider whether to add feed-forward capacitors according to the situation.

The use of a feed-forward capacitor (CFF) in the feedback network is to improve the transient response or higher phase margin. To reduce transient ripple, the feed-forward capacitor value can be increased to push the cross frequency to higher region. Although this can improve transient response, it also decreases phase margin and cause more ringing. In the other hand, if more phase margin is desired, the feed-forward capacitor value can be decreased to push the cross frequency to lower region.

the value of feed-forward capacitor (CFF) can be calculated with the following equation:

$$C_{ff\_op} = \frac{1}{2\pi \times f_{nocff}} \times \sqrt{\frac{1}{R_1} \times \left(\frac{1}{R_1} + \frac{1}{R_2}\right)}$$

Where F<sub>nocff</sub> is the cross frequency. the crossing frequency is generally taken as 1/10 to 1/5 of the switching frequency, R<sub>1</sub> and R<sub>2</sub> are feedback resistors.

### ● Bootstrap Capacitor Selection

Bootstrap Capacitor Selection A 0.1-μF ceramic capacitor must be connected between the VBST to SW pin for proper operation. recommends to use a ceramic capacitor.

### ● Setting current limit

A current sensing resistor R<sub>3</sub> can be used to adjust current limit. The following equation can be used to calculate the needed resistor value.

$$R_3 = \frac{0.9}{I_{load} \times 15} \Omega$$

● **Line drop compensation**

When USB charging cable line is long and resistance is high, there will be some significant voltage drop on the cable. Portable device will see much lower input voltage. If the voltage across the load input terminals is too low, it will affect the charge time for the load. It is recommended to adjust the output voltage of charger to compensate this voltage drop. DP31231C/B has an configurable line drop compensation feature. The line drop compensation value can be programmed by the top feedback resistor R1 in Fig 1. The line compensation voltage can be roughly calculated as following:

$$\Delta V_{out} = R_{cs} * I_{out} * 15 * R1 / 200k\Omega$$

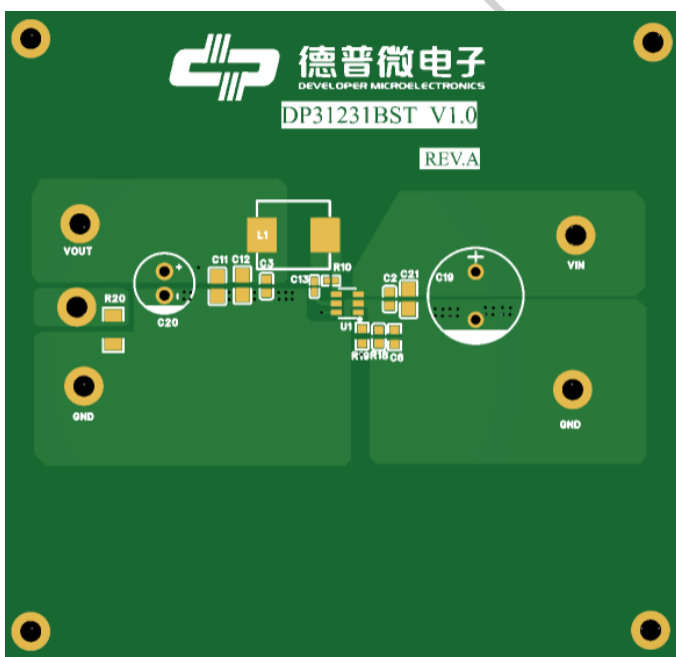
Rcs is the sum of current sensing resistor on CS pin, all of the parasitic resistance on PCB board and GND pin. Iout is output load current going through Rcs. R1 is the top feedback resistor

● **PCB Layout**

PCB layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion efficiency, thermal performance, and minimized EMI.

1. The feedback network, resistor R18 and R19, should be kept close to FB pin. Vout sense path

● **Layout Example:**



should stay away from noisy nodes, such as SW & BS signals and preferably through a layer on the other side of shielding layer.

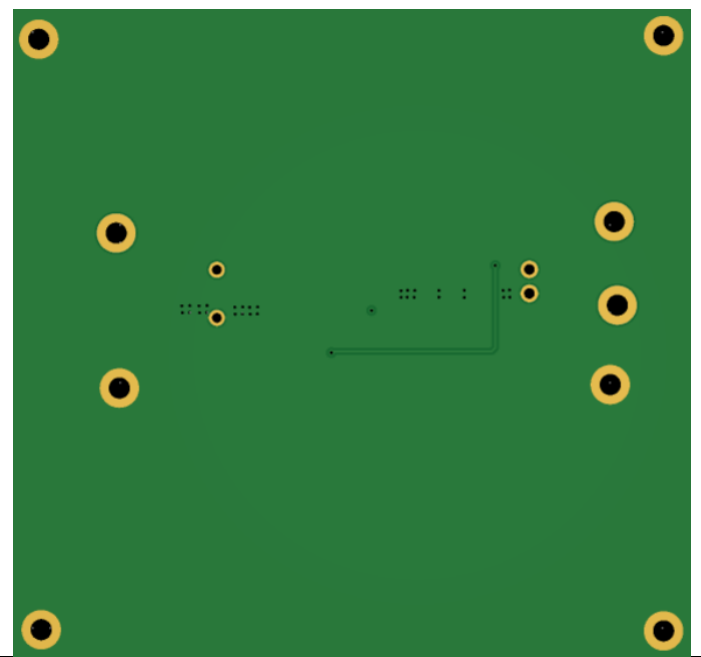
2. The input bypass capacitor C21 and C2 must be placed as close as possible to the VIN pin and ground. Grounding for both the input and output capacitors should consist of localized top side planes that connect to the GND pin and PAD. It is a good practice to place a ceramic cap near the VIN pin to reduce the high frequency injection current.

3. The inductor L should be placed close to the SW pin to reduce magnetic and electrostatic noise.

4. The output capacitor, COUT should be placed close to the junction of L1. The L1, and COUT trace should be as short as possible to reduce conducted and radiated noise and increase overall efficiency.

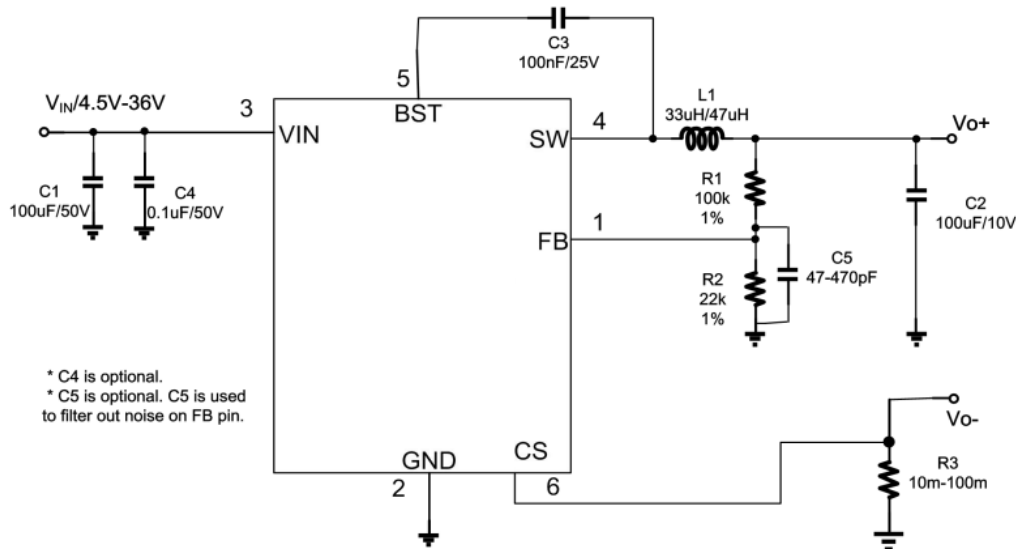
5. The ground connection for C21, C2 and C20, C11, C12 should be as small as possible and connect to system ground plane at only one spot (preferably at the COUT ground point) to minimize injecting noise into system ground plane.

6. Large GND Copper Pour near IC is recommended to minimize the heat of IC.

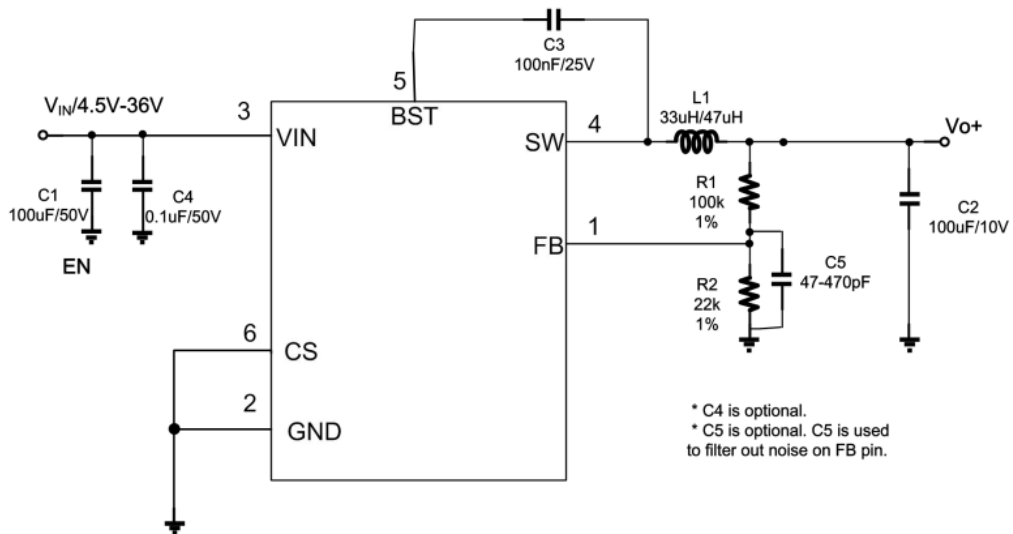




## Typical Application Schematic



Word Mode 1:CC/CV Mode CS to GND with sensing resistor

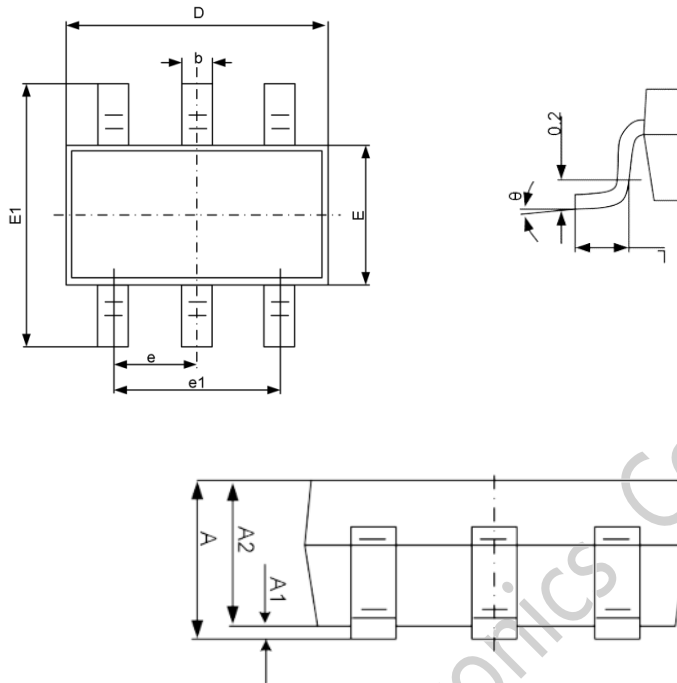


Word Mode 2:CV Mode CS to GND



PACKAGE DIMENSION

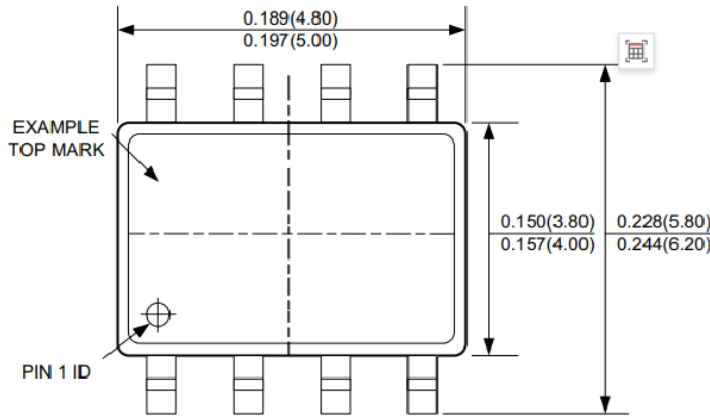
SOT23-6



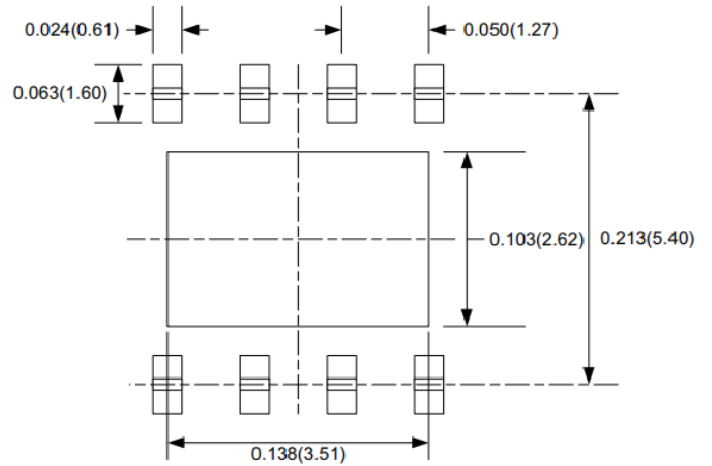
Symbol	Dimensions in Millimeters	
	Min	Max
A	-	1.350
A1	0.000	0.150
A2	1.000	1.200
b	0.300	0.500
c	0.100	0.220
D	2.820	3.020
E	1.500	1.700
E1	2.600	3.000
e	0.950(BSC)	
e1	1.800	2.000
L	0.300	0.600
$\theta$	0°	8°



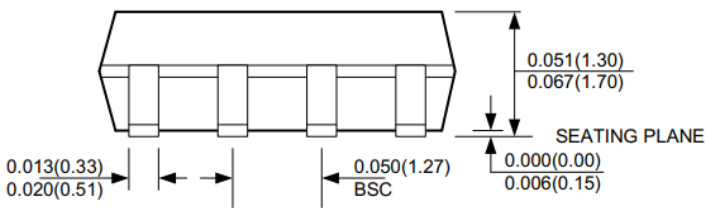
ESOP8 (EXPOSED PAD)



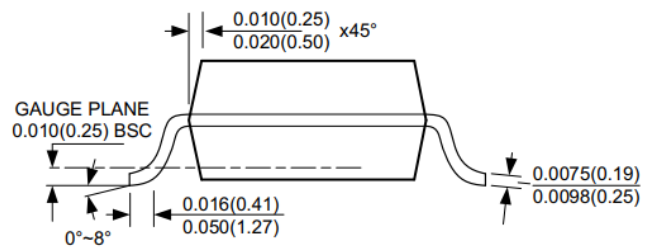
TOP VIEW



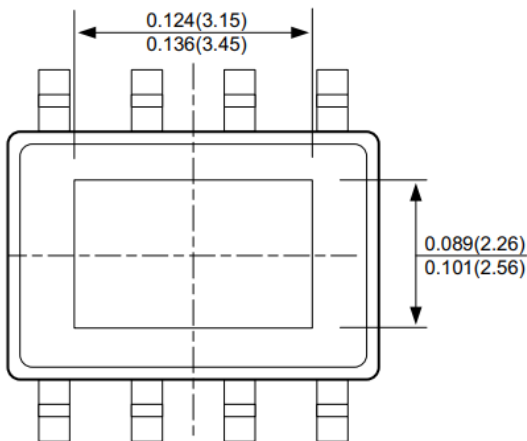
RECOMMENDED PAD LAYOUT



FRONT VIEW



SIDE VIEW



BOTTOM VIEW

NOTE:

1. CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2. PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5. DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6. DRAWING IS NOT TO SCALE.



## REVISION HISTORY

Editions	Revised Date	Redaction person	Revision content
A.0	2023/12/23	PXB	First release

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