36V, 2.4A CC&CV Step-Down Switching Regulator

FEATURES

- Up to 95% Efficiency
- Input Voltage Range: 6.5V to 30V
- Continuous Output Current: 2.4A
- switching frequency: 500KHZ
- Reference Voltage: 0.9V ±2% @25℃
- Maximum Duty Cycle: 96%
- Integrated 36V, 108mΩ high side and 36V, 102mΩ low side power MOSFET switches
- Pulse Skipping Mode to Achieve High Light Load Efficiency
- Frequency jittering to ease EMI Issue
- Peak Current-Mode Control
- Cycle-by-Cycle Over Current Protection
- Input over-voltage protection
- Output Over-Voltage Protection
- Output short protection
- Over-Temperature Protection
- Constant-On-Time Control scheme

DESCRIPTIONS

The DP31232E is a monolithic synchronous buck regulator with wide operating input voltage range from 6.5 to 36V. Current mode control with internal slope compensation is implemented to reduce component count. DP31232E also features a light load pulse skipping mode, which allows for a power loss reduction from the input power supply to the system at light loading. The switching frequency of the converters is Fix 500KHZ. Frequency spread spectrum operation is introduced for EMI reduction. A cycle-by-cycle current limit with frequency fold back protects the IC at over loading condition.DP31232E uses external compensation, This simplifies the loop design for different frequencies

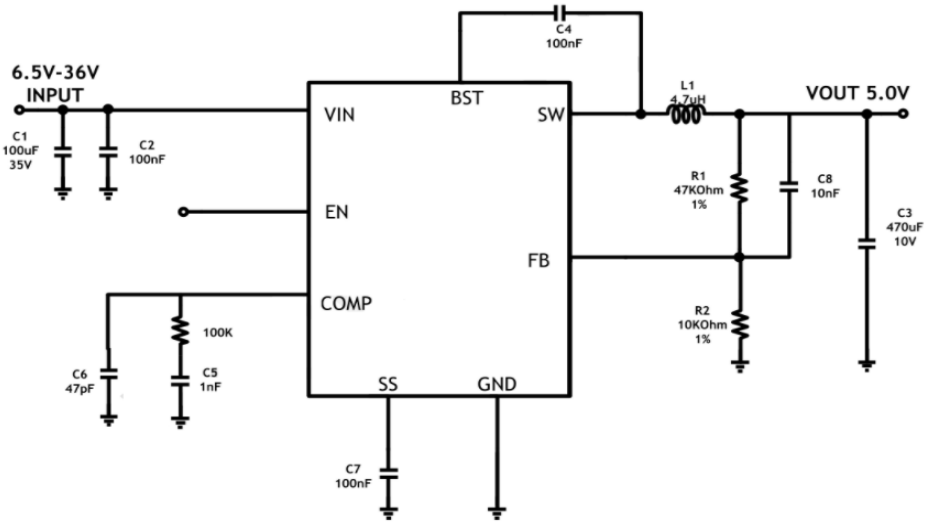
APPLICATIONS

- USB car charger
- Portable charging device
- General purpose DC-DC conversion

ORDERING INFORMATION

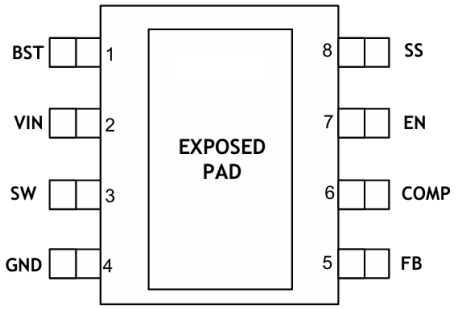
Part Number	Description
ESOP8	Pb free in T&R, 4000 Pcs/Reel

TYPICAL APPLICATION CIRCUIT



PRODUCT DESCRIPTION

➢ Pin Arrangement

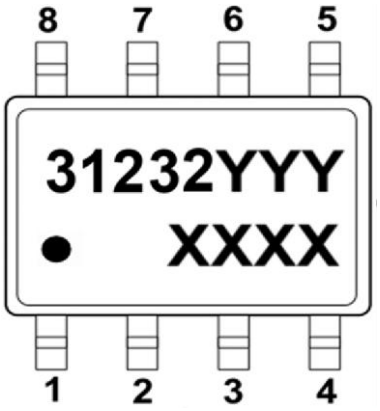


ESOP8

➢ Pin Configuration

ESOP8	Pin Name	Description
1	BST	Supply input for the high-side NFET gate drive circuit. Connect a 0.1μF capacitor between VBST and SW pins.
2	VIN	Power supply voltage input
3	SW	Switch pin connected to the internal FET switches and inductor terminal. Connect the inductor of the output filter to this pin.
4	GND	Ground Pin
5	FB	Feedback pin for the internal control loop. Connect this pin to an external feedback divider.
6	COMP	Error amplifier output and input to the PWM comparator. Connect frequency compensation components to this pin.
7	EN	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator; low to turn it off. EN is pulled to VIN internally by a large resistor.
8	SS	Soft start pin. An external capacitor connected to this pin sets the output rise time.
9	EP	Exposed Pad

➢ Marking Information



DP31232 for product name:

YYY refers to the following table description, represents different packaging and special functions

XXXX The first X represents the last year,2020 is 0;The second X represents the month,inA-L 12 letters;The third and fourth X on behalf of the date,01-31said;

Marking	Model	Description
31232E	DP31232ESO	DP31232ESO Buck，4.6V~36V，2.4A，VFB 0.9V，**DCM**，ESOP8

➢ Absolute Maximum Ratings

PARAMETER	Min	Max	Unit
VIN Voltage	-0.3	36	V
SW Voltage(DC)	-0.3	36	V
SW Voltage(AC less than 10ns while Switching)	-1	37	V
FB Voltage	-0.3	6	V
BS Voltage(vs SW)	-0.3	6	V
Other Voltage(SS\Comp)	-0.3	6	V
Operating junction temperature,TJ	-40	150	℃
Storage temperature, Tstg	-65	150	℃
Lead Temperature（Soldering，10sec.)	-	260	℃

Over operating temperature range (unless otherwise noted)(1)

Note:(1)Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute－maximum－rated conditions for extended periods may affect device reliability.

（2）All voltage values are with respect to network ground terminal

➢ Recommended Operating Conditions

PARAMETER	Min	Max	Unit
VIN Voltage(V_{IN})	6.5	30	V
Output current	0	2.4	A
TJ	-40	125	℃

Note : (1)All limits specified at room temperature (TA = 25°C) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

ESD Ratings

PARAMETER	Description	Value	Unit
HBM	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
CDM	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±200	V

Note : (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

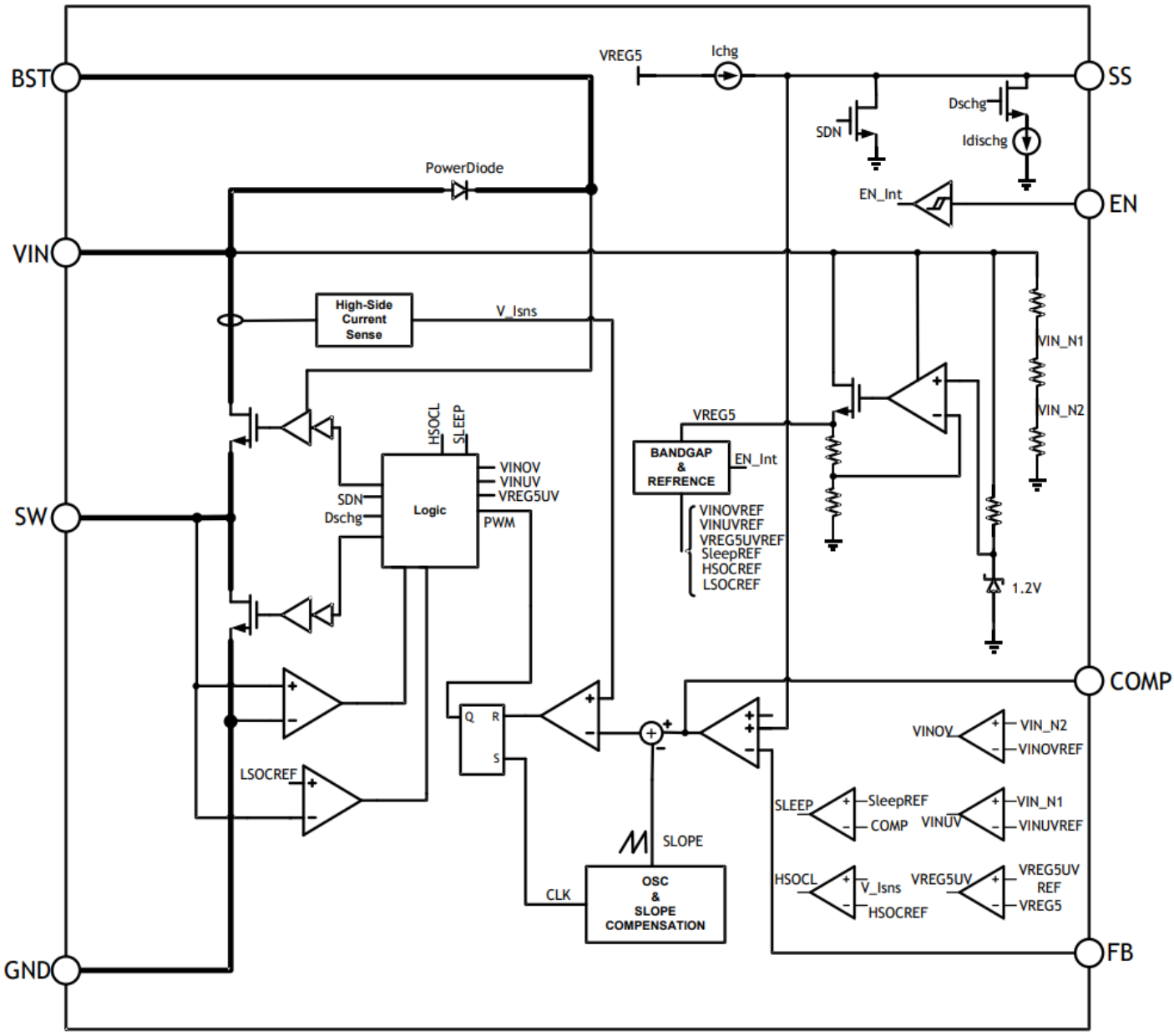
➢ Thermal Information

THERMAL METRIC	Description	ESOP8	Unit
RθJA	Junction-to-ambient thermal resistance(1)(2)	48.7	℃/W
RθJC(top)	Junction-to-case (top) thermal resistance	52.4	℃/W
RθJB	Junction-to-board(Bottom) thermal resistance	25.5	℃/W
ψJT	Junction-to-top characterization parameter	8.4	℃/W
ψJB	Junction-to-board characterization parameter	25.2	℃/W

Note (1): The package thermal impedance is calculated in accordance to JESD 51-7.

Note (2): Thermal Resistances were simulated on a 4-layer, JEDEC board

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS(Typical at Vin=12V,TJ=25°C, unless otherwise noted.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Buck Input Standoff Voltage	$V_{IN(max)}$		36			V
Input Voltage	V_{IN}		6.5		30	V
Input Over Voltage	V_{IN_OVP}			33		V
VIN UVLO Rising Threshold	$V_{UVLO(R)}$	V_{IN} Rising		6.37		V
VIN UVLO Falling Threshold	$V_{UVLO(F)}$	V_{IN} Falling		6		V
VIN UVLO Hysteresis	$V_{UVLO(HYS)}$			0.37		V
FB Voltage	V_{FB}	T_J=25℃		0.9		V
FB Leakage Current	$I_{FB(LkG)}$	T_J=25℃	-100	10	100	nA
Switching Frequency	Fsw			500		KHZ
Max duty cycle	Dmax				96	%
Mini on Pulse Width	$T_{ON(MIN)}$			100		ns
High-Side Switch Current Limit	$I_{HS(OC)}$	V_{IN}= 48V, V_{FB}=90%		4.5		A
High-Side MOS ON-Resistance	$R_{DSON(HS)}$	Isw=100mA		108		mΩ
Low-Side MOS ON-Resistance	$R_{DSON(LS)}$	Isw=100mA		102		mΩ
VOUT OVP	V_{OUT_OVP}			1.1*FB		V
EN Rising Threshold	$V_{EN(R)}$	EN Rising	1.2			V
EN Falling Threshold	$V_{EN(F)}$	EN Falling			1	V
Soft-Start Period	Tss			0.5		ms
Comp Source Current	Icmp_src	VFB = 1.0 V		60		uA
Comp Sink Current	Icmp_snk	VFB = 0.8 V		60		uA
COMP to current sense transconductance	Gm_PS			5		A/V
EN Hysteresis	$V_{EN(HYS)}$			0.2		V
Over-Temperature Protection	T_{SD}			155		℃
Over-Temperature Protection hysteresis	$\triangle T_{SD}$			30		℃

TYPICAL CHARACTERISTICS

Test Condition: TA = 25℃, VIN=12V, Vout=5V, unless otherwise noted.

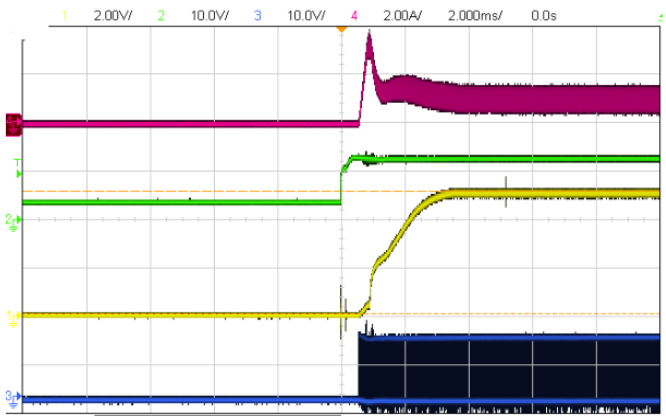


Figure1 VIN StartUp with Iout=1A

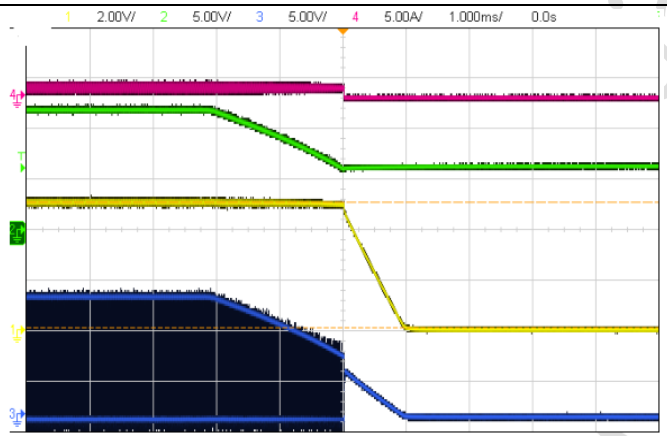


Figure2 ShutDown with Iout=2A

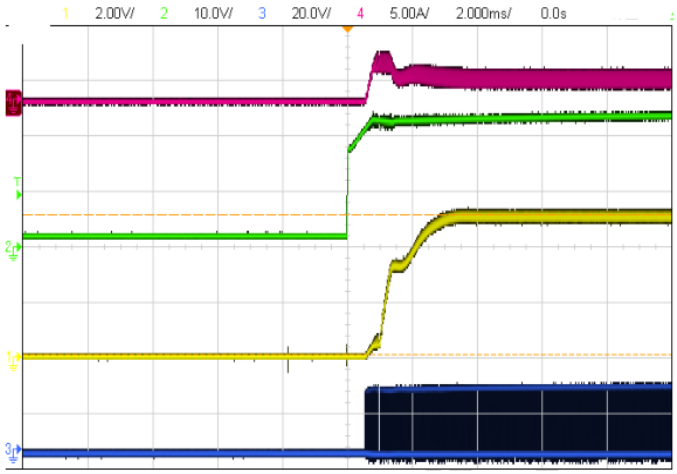


Figure3 VIN StartUp with 2A Load

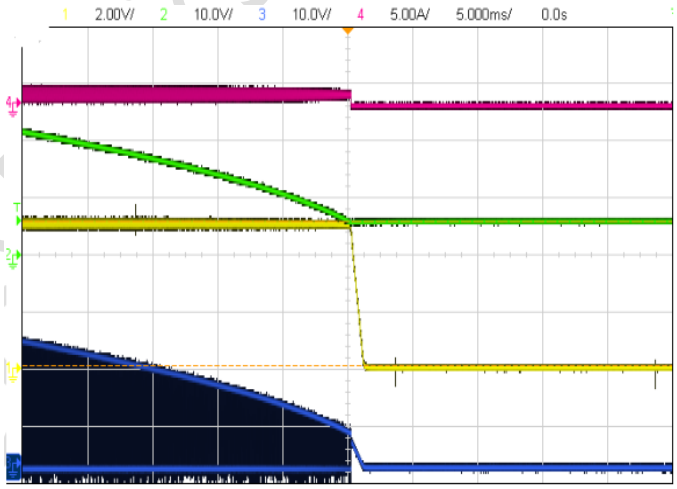


Figure4 VIN ShutDown with 2A Load

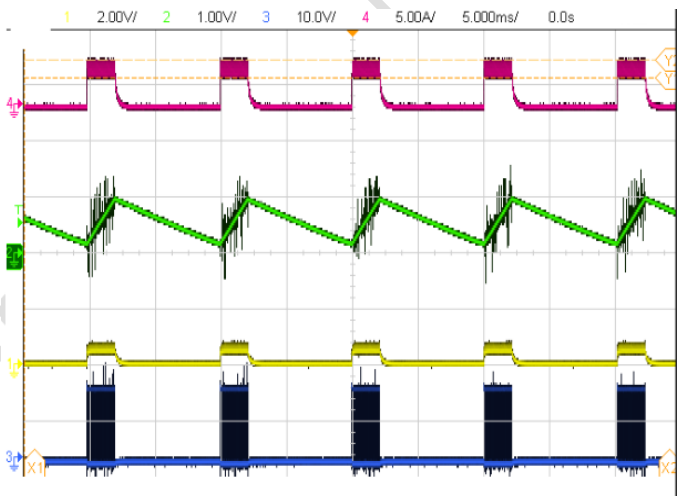


Figure5 VIN=12V Short Protection Wavefrom

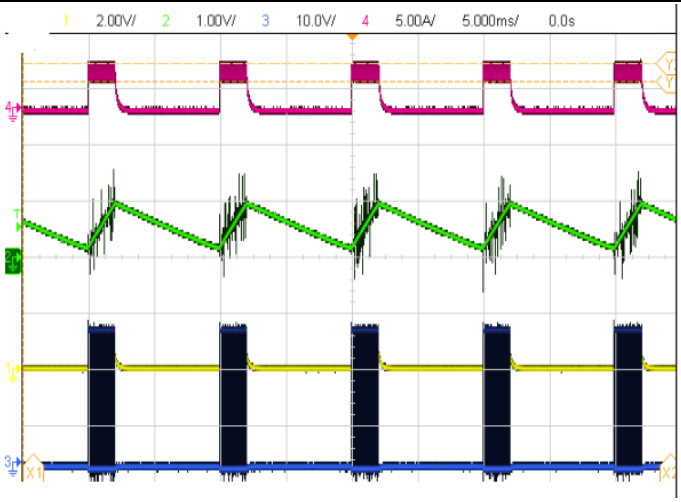


Figure6 VIN=24V Short Protection Wavefrom

FUNCTIONS DESCRIPTION

- **Feature Description**

The DP31232E is a COT mode step down DC/DC converter that provides excellent transient response with no extra external compensation components. This device contains an internal, low resistance, high voltage power MOSFET, Switching frequency is internally.

- **Thermal Shutdown**

The internal thermal-shutdown circuitry forces the device to stop switching if the junction temperature exceeds 160 ° C typically. Once the junction temperature falls below the falling threshold, the device returns to normal operation automatically.

- **Soft Start**

The soft-start is implemented to prevent the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) ramping up from 0V to 0.9V. When it is lower than the internal reference (REF), SS overrides REF so the error amplifier uses SS as the reference. When SS is higher than REF, REF regains control. The SS time is internally max to 0.5ms.

- **UNDER-VOLTAGE LOCKOUT (UVLO)**

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. When the voltage is higher than UVLO threshold voltage, the device is enabled again.

- **Startup AND Shutdown**

The If both VIN and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first,generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries. Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering.The comp voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

- **Over current and Short Circuit Protection**

The DP31232E has cycle-by-cycle over current limit when the inductor current peak value exceeds the set current limit threshold. Meanwhile, output voltage starts to drop until FB is below the Under-Voltage (UV) threshold. When the output is shorted to the ground, the switching frequency is Hiccup mode and the current limit is reduced to lower the short circuit current. The frequency Hiccup helps prevent inductor current runaway and thermal issue during short circuit. The DP31232E exits the hiccup mode once the over current condition is removed.

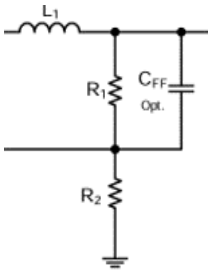
APPLICATION INFORMATION

The output stage of Asynchronous buck converter is mainly composed of inductor and capacitors. By switching the internally integrated High Side power MOSFET, the energy is stored and transferred to the load, and the second-order LC filter is formed to smooth the switching node voltage so that the stable output DC voltage is obtained.

- **Setting Output Voltage**

The output voltage is set by FB voltage, which is divided by resistor (R1 & R2) from output node to Ground. That resistor with 1% or higher accuracy is preferred. The output voltage value is set by equation as below.

$V_{OUT}=V_{FB} \times ((R1+R2)/R2)$



Vref is the internal reference voltage of DP31232E, 0.9V.

- **Inductor selection**

An inductor is required to supply constant current to the load while being driven by the switched input voltage. The common value of the inductance is between 22uH to 33uH. A larger value inductor will result in less current ripple and lower output voltage ripple. However, the larger value inductor will have larger physical size, higher DC resistance, and/or lower saturation current. A good rule to calculate the inductance is to allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum load current. At the same time, it is needed to make sure that the peak inductor current is below the inductor saturation current.

The inductance value can be calculated by:

$$L=\frac{V_{OUT}}{f_s \times \Delta I_L}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

Where VOUT is the output voltage, VIN is the input voltage, fs is the switching frequency, and ΔL is the peak-to-peak inductor ripple current.

The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

The choice of which style inductor to use mainly depends on the price vs. size requirements and any EMI constraints.

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency

- **Input capacitors selection**

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the converter. It is recommend to use low ESR capacitors to optimize the performance. Ceramic capacitor is preferred, but tantalum or low-ESR electrolytic capacitors may also meet the requirements. It is better to choose X5R or X7R dielectrics when using ceramic capacitors.

Since the input capacitor (CIN) absorbs the input switching current, a good ripple current rating is required for the capacitor. The RMS current in the input capacitor can be estimated by:

$$I_{CIN}=I_{load} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1-\frac{V_{OUT}}{V_{IN}}\right)}$$

The worst-case condition occurs at VIN = 2×VOUT, where:

$$I_{CIN}=\frac{I_{load}}{2}$$

For simplification, choose the input capacitor whose RMS current rating is greater than half of the

maximum load current. When electrolytic or tantalum capacitors are used, a small, high quality ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible. When ceramic capacitors are used, make sure that they have enough capacitance to maintain voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN}=\frac{I_{load}}{f_s\times C_{IN}}\times\frac{V_{OUT}}{V_{IN}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

CIN is the input capacitance.

- **Output capacitors selection**

The output capacitor (COUT) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT}=\frac{V_{OUT}}{f_s\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times\left(R_{ESR}+\frac{1}{8\times f_s\times C_{OUT}}\right)$$

Where L is the inductor value, RESR is the equivalent series resistance (ESR) value of the output capacitor and COUT is the output capacitance value. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly determined by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT}=\frac{V_{OUT}}{8\times f_s^{2}\times L\times C_{OUT}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT}=\frac{V_{OUT}}{f_s\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The DP31212S/FS can be optimized for a wide range of capacitance and ESR values.

- **Feed-Forward Capacitor Selector(CFF)**

DP31232E has internal loop compensation, so adding CFF is optional. Specifically, consider whether to add feed-forward capacitors according to the situation.

The use of a feed-forward capacitor (CFF) in the feedback network is to improve the transient response or higher phase margin. To reduce transient ripple, the feed-forward capacitor value can be increased to push the cross frequency to higher region. Although this can improve transient response, it also decreases phase margin and cause more ringing. In the other hand, if more phase margin is desired, the feed-forward capacitor value can be decreased to push the cross frequency to lower region.

the value of feed-forward capacitor (CFF) can be calculated with the following equation:

$$Cff\_op=\frac{1}{2\pi\times f_{\_nocff}}\times\sqrt{\frac{1}{R1}\times\left(\frac{1}{R1}+\frac{1}{R2}\right)}$$

Where F_nocff is the cross frequency. the crossing frequency is generally taken as 1/10 to 1/5 of the switching frequency, R1 and R2 are feedback resistors.

- **Bootstrap Capacitor Selection**

The recommended capacitor is 0.1 μF and rated 16 V or higher. The bootstrap capacitor is located between the SW pin and the BOOT pin. The bootstrap capacitor must be a high-quality ceramic type with an X7R or X5R grade dielectric for temperature stability.

- **PCB Layout**

PCB layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion efficiency, thermal performance, and minimized EMI.

1. The feedback network, resistor R7 and R8, should be kept close to FB pin. Vout sense path should stay away from noisy nodes, such as SW & BS signals and preferably through a layer on the other side of shielding layer.

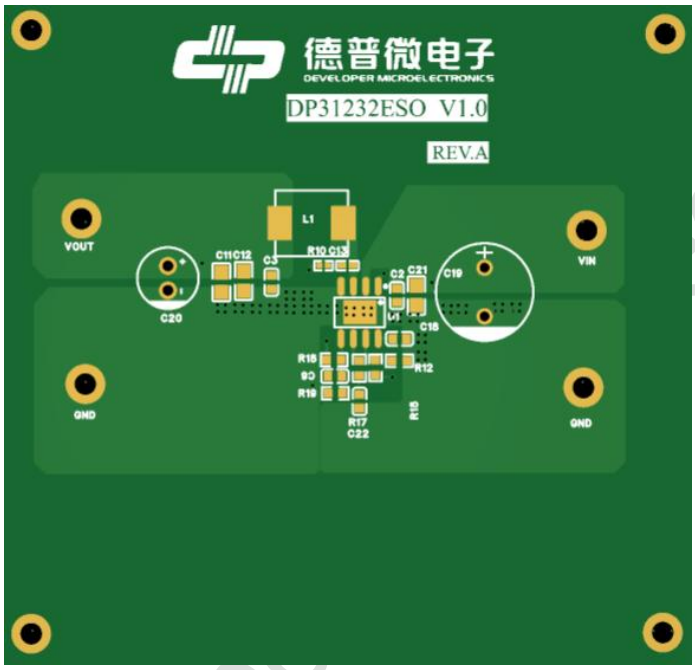
2. The input bypass capacitor C21 and C2 must be placed as close as possible to the VIN pin and ground. Grounding for both the input and output capacitors should consist of localized top side planes that connect to the GND pin and PAD. It is a good practice to place a ceramic cap near the VIN pin to reduce the high frequency injection current.

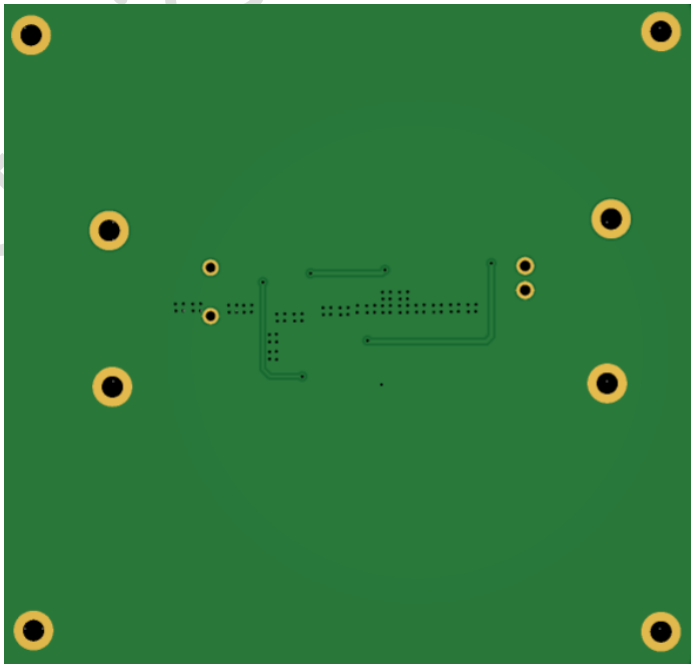
3. The inductor L should be placed close to the SW pin to reduce magnetic and electrostatic noise.

4. The output capacitor, COUT should be placed close to the junction of L and the diode D. The L, D, and COUT trace should be as short as possible to reduce conducted and radiated noise and increase overall efficiency.

5. The ground connection for C21,C19,C2 and C11 ,C3,C12 should be as small as possible and connect to system ground plane at only one spot (preferably at the COUT ground point) to minimize injecting noise into system ground plane.

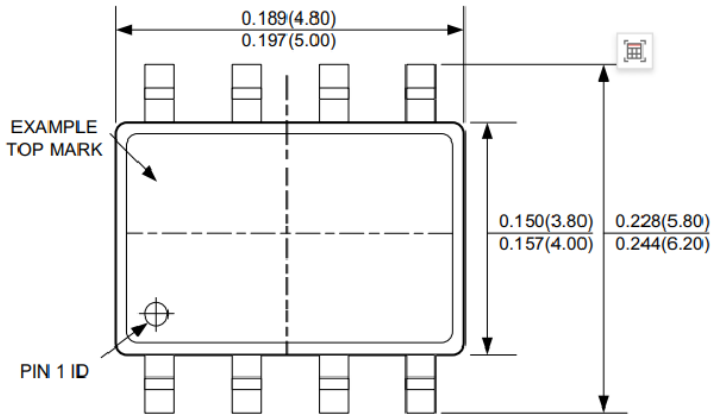
6. Large GND Copper Pour near IC is recommended to minimize the heat of IC.



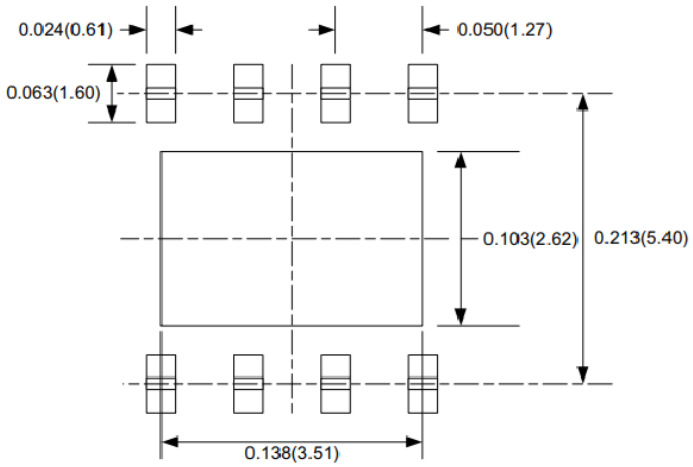


PACKAGE DIMENSION

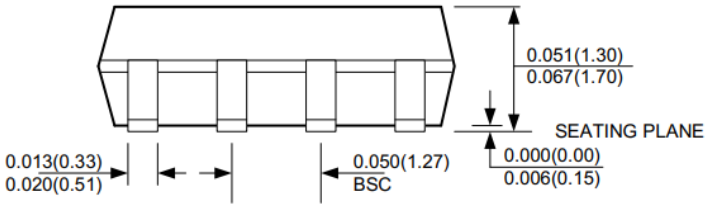
ESOP8 (EXPOSED PAD)



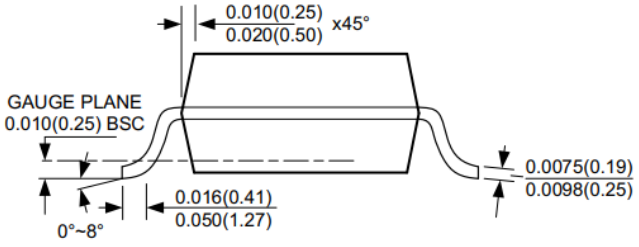
TOP VIEW



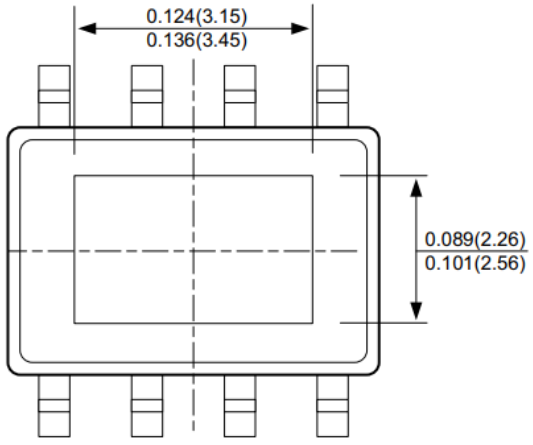
RECOMMENDED PAD LAYOUT



FRONT VIEW



SIDE VIEW



BOTTOM VIEW

NOTE:
1. CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2. PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5. DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6. DRAWING IS NOT TO SCALE.

REVISION HISTORY

Editions	Revised Date	Redaction person	Revision content
A.0	2023/12/23	PXB	First release

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