4.8V to 60V Input, 5A synchronous Buck Converter

FEATURES

- Up to 95% Efficiency
- Input Voltage Range: 4.8V to 60V
- Continuous Output Current: 5A
- Adjustable switching frequency range: Up to 2MHZ
- Reference Voltage: 0.8V ±1% @25℃
- Maximum Duty Cycle: 100%
- Integrated high-side MOSFET:80mΩ
- Low Quiescent Current: 175μA
- Low Shutdown Current: 10μA
- Optional Operation Modes at Light-Load
- Over Current Protection
- 68V Input over voltage protection
- Fixed 3ms Internal soft start timer
- Short Protection with Hiccup-Mode
- Thermal Shutdown Protection

APPLICATIONS

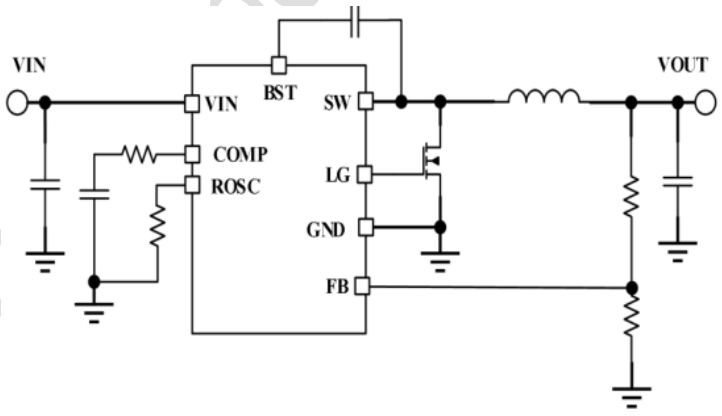
- POE
- Appliances, power and garden tools
- High-cell-count battery packs (E-Bike, E-Scooter)
- Motor drives, drones, telecom
- Industrial Automation and Motor Control
- USB Dedicated Charging Ports and Battery Chargers
- Vehicle Accessories: GPS, Entertainment

DESCRIPTIONS

The DP31265A is a 60V, 5A, Synchronous step down regulator with an integrated high side MOSFET. The device survives load dump pulses up to 68V. Current mode control provides simple external compensation and flexible component selection. A low ripple pulse skip mode reduces the no load supply current.

Under voltage lockout is internally set at 4.8V . The output voltage start up ramp is internally controlled to provide a controlled startup and eliminate overshoot. A wide switching frequency range allows either efficiency or external component size to be optimized. Output current is limited cycle-by-cycle. Frequency fold-back and thermal shutdown protects internal and external components during an overload condition. Additional features of the DP31265A include ultra low IQ and high light load efficiency, innovative peak current protection, integrated VCC bias supply and bootstrap diode, precision enable and input UVLO, and thermal shutdown protection with automatic recovery.

TYPICAL APPLICATION CIRCUIT

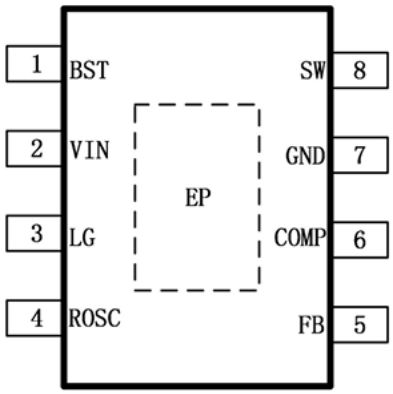


ORDERING INFORMATION

Part Number	Description
ESOP8	Pb free in T&R, 4000 Pcs/Reel

PRODUCT DESCRIPTION

➢ Pin Arrangement



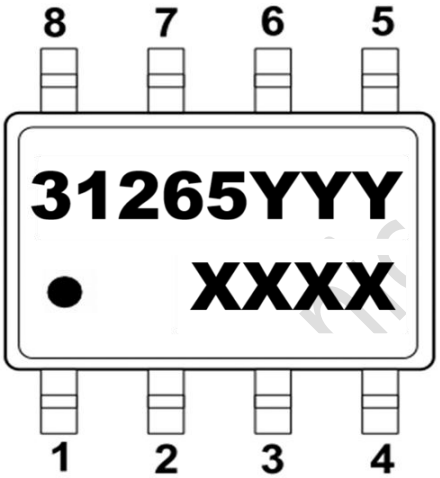
ESOP8

➢ Pin Configuration

ESOP8	Pin Name	Description
1	BST	Supply input for the high-side NFET gate drive circuit. Connect a 0.1μF capacitor between VBST and SW pins.
2	VIN	Power supply voltage input
3	LG	Output driver for low side MOSFET.
4	ROSC	Resistor Timing. An internal amplifier holds this terminal at a fixed voltage when using an external resistor to ground to set the switching frequency. If the terminal is pulled above the PLL upper threshold, a mode change occurs and the terminal becomes a synchronization input. The internal amplifier is disabled and the terminal is a high impedance clock input to the internal PLL. If clocking edges stop, the internal amplifier is re-enabled and tha operating mode returns to resistor frequency programming.
5	FB	Feedback pin for the internal control loop. Connect this pin to an external feedback divider.
6	COMP	Error amplifier output and input to the output switch current (PWM) comparator. Connect frequency compensation components to this terminal.
7	GND	Ground Pin
8	SW	The source of the internal high-side power MOSFET and

		switching node of the converter.
9	EP	Exposed pad of the package. No internal electrical connection. Solder the EP to the GND pin and connect to a large copper plane to reduce thermal resistance.

➢ Marking Information



DP31265 for product name:

YYY refers to the following table description, represents different packaging and special functions

XXXX The first X represents the last year,2020 is 0;The second X represents the month,inA-L 12 letters;The third and fourth X on behalf of the date,01-31said;

Marking	Model	Description
31265A	DP31265ASO	DP31265ASO Buck Converter，4.8V~60V，5A，VFB 0.8V， ESOP8

➢ Absolute Maximum Ratings

PARAMETER	Min	Max	Unit
VIN Voltage	-0.3	80	V
EN Voltage	-0.3	6.5	V
SW Voltage(DC)	-0.3	80	V
SW Voltage(AC less than 10ns while Switching)	-1.5	80	V
FB Voltage	-0.3	6.5	V
BS Voltage(vs SW)	-0.3	8	V
COMP to GND	-0.3	6.5	V
Operating junction temperature,TJ	-40	150	℃
Storage temperature, Tstg	-65	150	℃
Lead Temperature（Soldering，10sec.)	-	260	℃

Over operating temperature range (unless otherwise noted)(1)

Note:(1)Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute－maximum－rated conditions for extended periods may affect device reliability.

（2）All voltage values are with respect to network ground terminal

➢ Recommended Operating Conditions

PARAMETER	Min	Max	Unit
VIN Voltage(V_{IN})	5	60	V
Output current	0	5	A
TJ	-40	125	℃

Note : (1)All limits specified at room temperature (TA = 25°C) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

ESD Ratings

PARAMETER	Description	Value	Unit
HBM	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
CDM	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±200	V

Note : (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

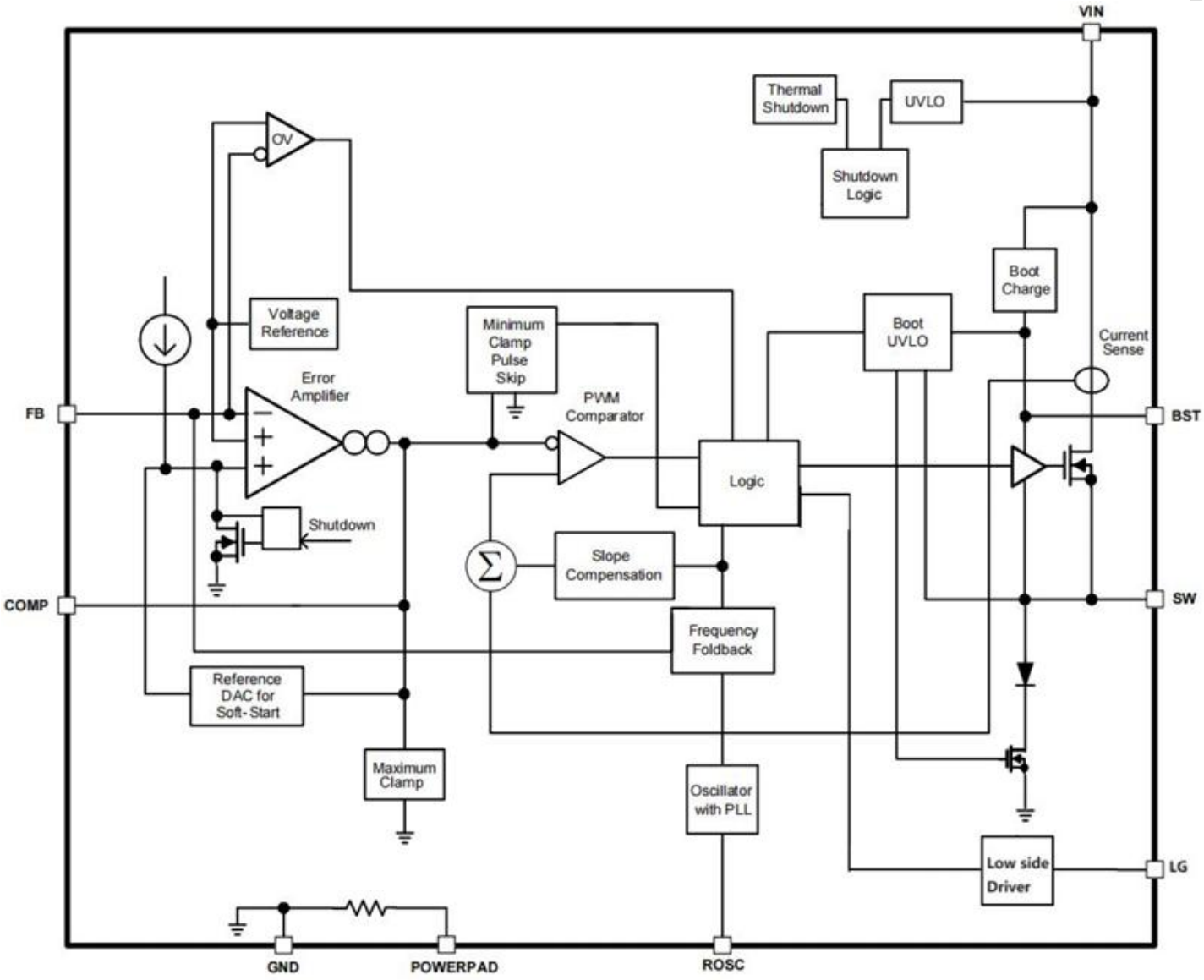
➢ Thermal Information

THERMAL METRIC	Description	ESOP8	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)(2)	48.7	℃/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.4	℃/W
$R_{\theta JB}$	Junction-to-board(Bottom) thermal resistance	25.5	℃/W
ψ_{JT}	Junction-to-top characterization parameter	8.4	℃/W
ψ_{JB}	Junction-to-board characterization parameter	25.2	℃/W

Note (1): The package thermal impedance is calculated in accordance to JESD 51-7.

Note (2): Thermal Resistances were simulated on a 4-layer, JEDEC board

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

(Typical at Vin=24V, VEN=2V，TJ=25°C, unless otherwise noted.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input Voltage	VIN		4.8		60	V
VIN Quiescent Current	IQ	No-switching，VFB=0.9V		930		uA
Shutdown Current	ISHDN	VEN=0V		10	15	uA
VIN UVLO Rising Threshold	VUVLO(R)	VIN Rsing			4.5	V
FB Voltage	VFB	TJ=25℃	0.792	0.8	0.808	V
EA Input Current	ECurrent		50			nA
EA DC Gain	EGain	VFB=0.8V	10000			V/V
Min unity gain bandwidth			2500			KHZ
EA Source/Sink		V(comp)=1V,100mV Over Drive	±30			uA
Low Side ILDRV		Peak Source Current		0.37		A
		Peak Sink Current		1.15		A
Low Side_rising time	Tr(LDRV)	CLOAD = 1000pF		40		ns
Low Side_falling time	Tf(LDRV)	CLOAD = 1000pF		20		ns
Switching Frequency For RT Mode	Fsw		100		2000	KHZ
		RSOC=22KΩ		330		KHZ
Switching Frequency For CLK Mode	FSW_CLK		160		2000	KHZ
ROSC/CLK high threshold	VROSC_High		1.55		2	V
ROSC/CLK Low threshold	VROSC_Low		0.5		1.2	V
Max duty cycle	Dmax				98	%
Current Limit Threshold	IHS(OC)	All VIN and temperatures, Open Loop		7.5		A
	IHS(OC)	VIN= 12V, Open Loop		5.5		A
High-Side MOS ON-Resistance	$R_{DSON(HS)}$	VIN=12V BS-SW=6V		80		mΩ
EN Rising Threshold	VEN(R)	EN Rising	1.1	1.2	1.3	V
Soft Start	Tss	10%*Vout to 90%*Vout		3		ms
Over-Temperature Protection	TSD			165		℃
Over-Temperature Protection hysteresis	△TSD			40		℃

TYPICAL CHARACTERISTICS

Test Condition：TA = 25℃，VIN=54V，Vout=12V，unless otherwise noted.

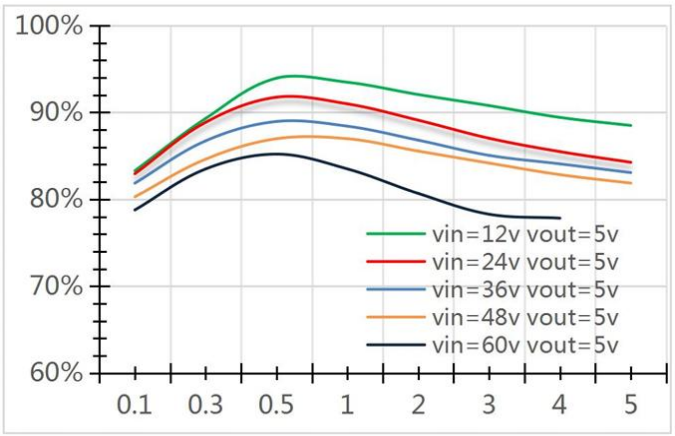


Figure1 5V Output Efficiency

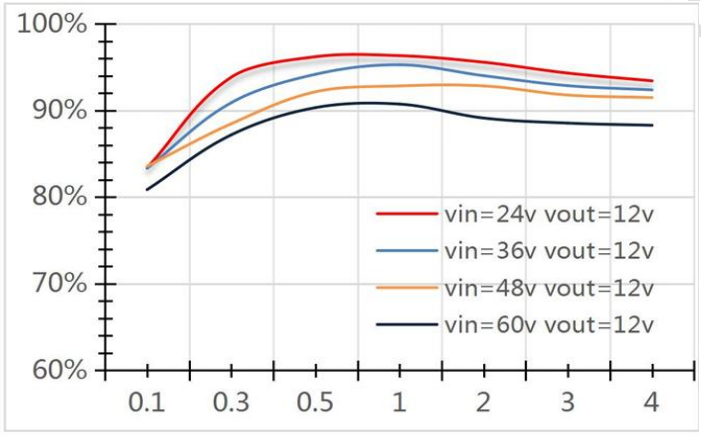


Figure2 12V Output Efficiency

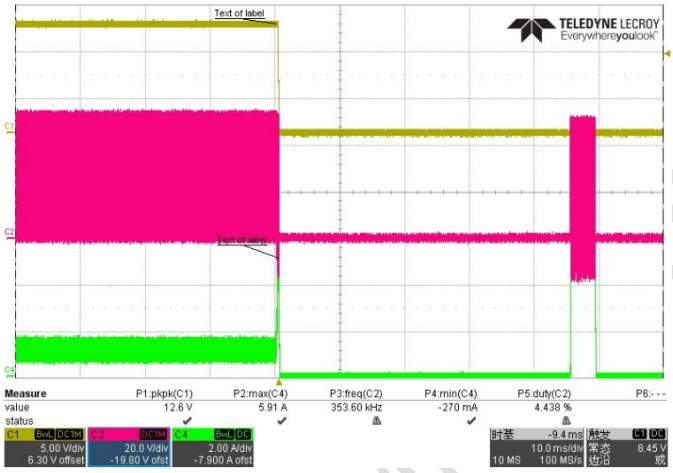


Figure3 12V Enter Short Circuit Wavefrom

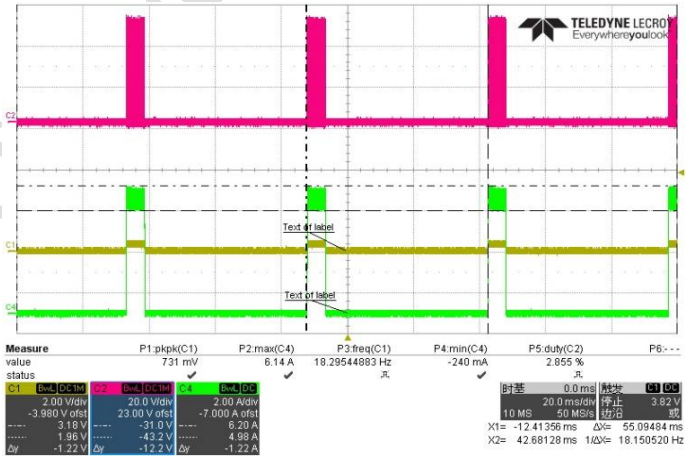


Figure4 Short Circuit wavefrom

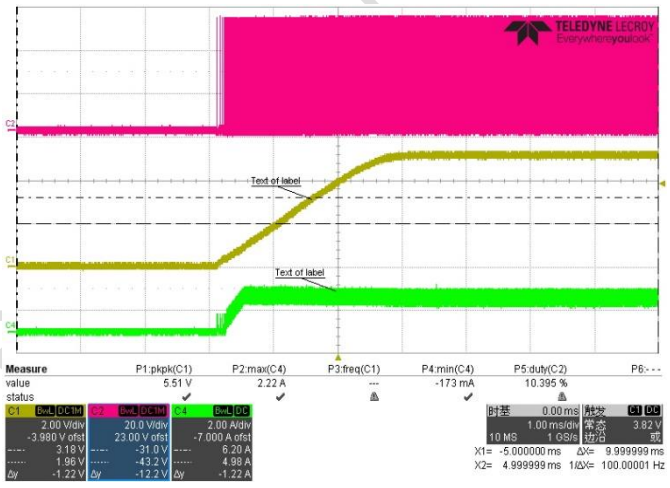


Figure5 Short Recovery Wavefrom

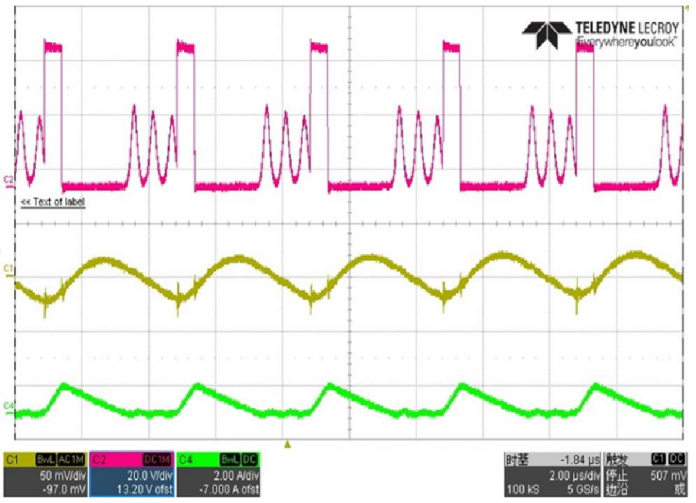


Figure6 DCM with Iout=0.1A

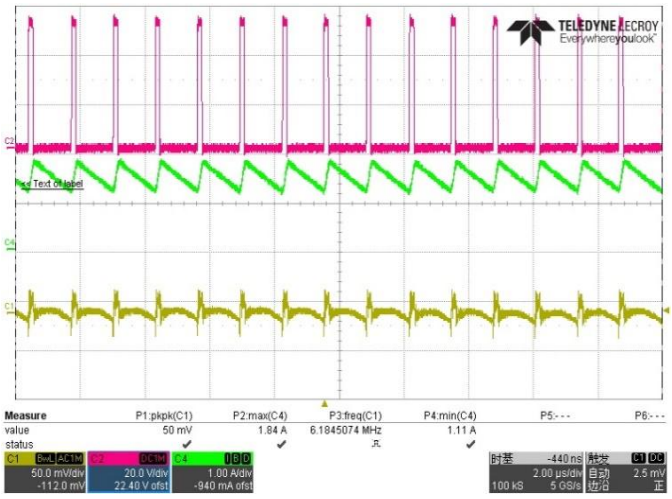


Figure7 CCM with Iout=1.5A

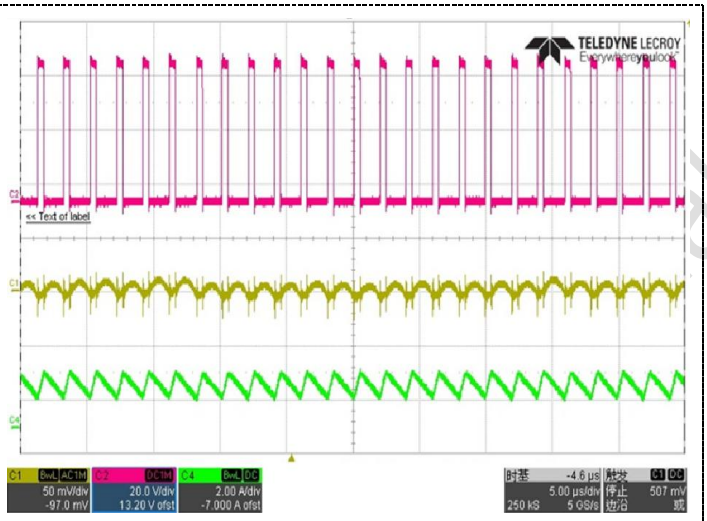


Figure8 CCM with Iout=3A

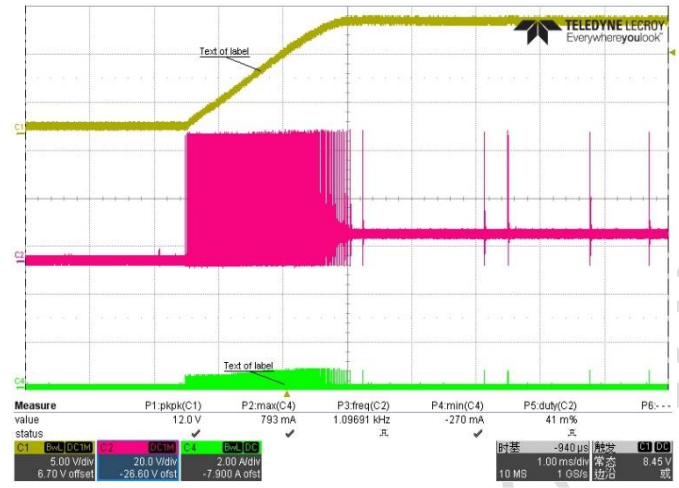


Figure9 VIN StartUp with No Load

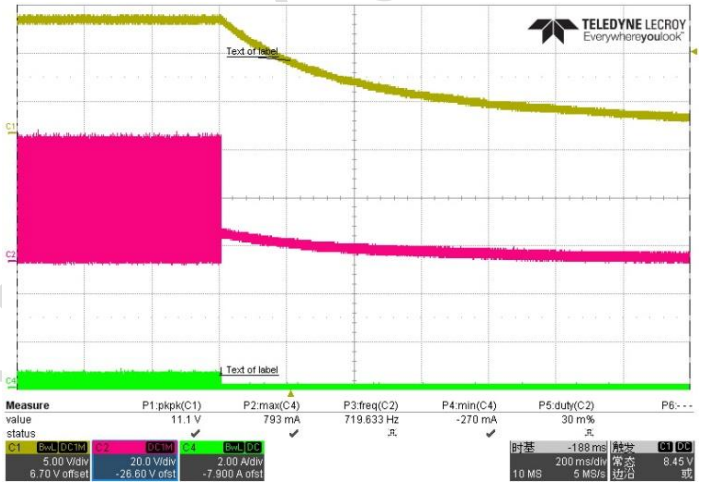


Figure10 ShutDown with No Load

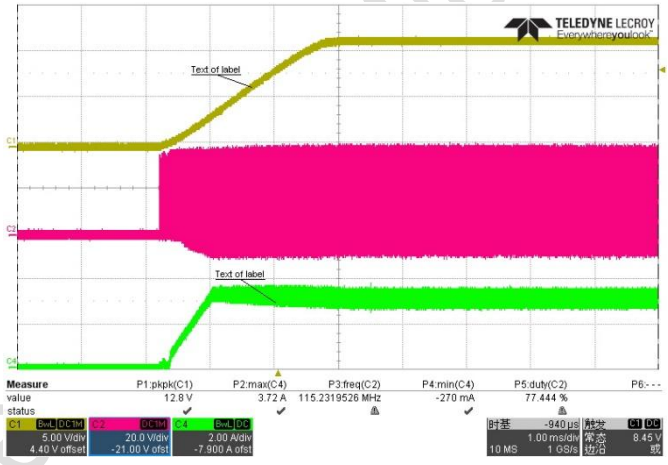


Figure11 VIN StartUp with 3A Load

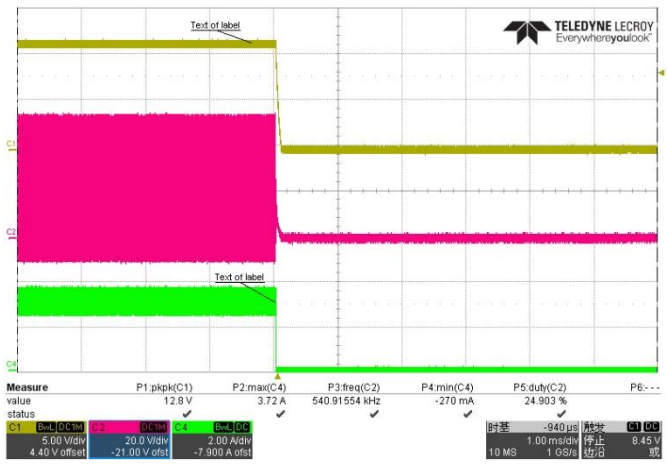


Figure12 VIN ShutDown with 3A Load

FUNCTIONS DESCRIPTION

- **Feature Description**

The DP31265A is a 60V, 5A, step-down (buck) regulator with an integrated high side n-channel MOSFET. The device implements constant frequency, current mode control which reduces output capacitance and simplifies external frequency compensation. The wide switching frequency range of 100 kHz to 2000 kHz allows either efficiency or size optimization when selecting the output filter components. The switching frequency is adjusted using a resistor to ground connected to the ROSC terminal. The device has an internal phase-locked loop (PLL) connected to the ROSC terminal that will synchronize the power switch turn on to a falling edge of an external clock signal.

- **Thermal Shutdown**

The DP31265A provides an internal thermal shutdown to protect the device when the junction temperature exceeds 175°C. The high side MOSFET stops switching when the junction temperature exceeds the thermal trip threshold. Once the die temperature falls below 164°C, the device reinitiates the power up sequence controlled by the internal soft-start circuitry.

- **Soft Start**

The soft-start is implemented to prevent the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) ramping up from 0V to 0.8V. When it is lower than the internal reference (REF), SS overrides REF so the error amplifier uses SS as the reference. When SS is higher than REF, REF regains control. The SS time is internally max to 3ms.

- **UNDER-VOLTAGE LOCKOUT (UVLO)**

The DP31265A is enabled when the VIN terminal voltage rises above 5.0V and the EN terminal voltage exceeds the enable threshold of 1.2V. The DP31265A is disabled when the VIN terminal voltage falls below 4.5V or when the EN terminal voltage is below 1.2V. The EN terminal has an internal pull-up current source of 1.2uA that enables operation of the DP31265A when the EN terminal floats

- **Adjustable Switching Frequency**

Determine the RROSC resistor using Equation 2 to set a specific switching frequency in CCM.

$$F_{SW}(kHz) = \frac{7095}{R_{ROSC}(k\Omega)} \quad (2)$$

- **Overvoltage Protection**

The DP31265A incorporates an output overvoltage protection (OVP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients in designs with low output capacitance. For example, when the power supply output is overloaded the error amplifier compares the actual output voltage to the internal reference voltage. If the FB terminal voltage is lower than the internal reference voltage for a considerable time,the output of the error amplifier will increase to a maximum voltage corresponding to the peak current limit threshold. When the overload condition is removed, the regulator output rises and the error amplifier output transitions to the normal operating level. In some applications, the power supply output voltage can increase faster than the response of the error amplifier output resulting in an output overshoot. The OVP feature minimizes output overshoot when using a low value output capacitor by comparing the FB terminal voltage to the rising OVP threshold which is nominally 109% of the internal voltage reference. If the FB terminal voltage is greater than the rising OVP threshold, the high side MOSFET is immediately disabled to minimize output overshoot. When the FB voltage drops below the falling OVP threshold which is nominally 106% of the internal voltage reference, the high side MOSFET resumes normal operation.

- **ERROR Amplifer**

The DP31265A voltage regulation loop is controlled by a transconductance error amplifier. The error amplifier compares the FB terminal voltage to the lower of the internal soft-start voltage or the internal 0.8V voltage reference. The transconductance (gm) of the error amplifier is 350μA/V during normal operation. During soft- start operation, the transconductance is reduced to 78μA/V and the error amplifier is referenced to the internal soft-start voltage. The frequency compensation components (capacitor, series resistor and capacitor) are connected between the error amplifier output COMP terminal and GND terminal

- **Fixed Frequency PWM Control**

The DP31265A uses fixed frequency, peak current mode control with adjustable switching frequency. The output voltage is compared through external resistors connected to the FB terminal to an internal voltage reference by an error amplifier. An internal oscillator initiates the turn on of the high side power switch. The error amplifier output at the COMP terminal controls the high side power switch current. When the high side MOSFET switch current reaches the threshold level set by the COMP voltage, the power switch is turned off. The COMP terminal voltage will increase and decrease as the output current increases and decreases. The device implements current limiting by clamping the COMP terminal voltage to a maximum level. The pulse skipping Eco-mode is implemented with a minimum voltage clamp on the COMP terminal.

- **Slope Compensation Output Current**

The DP31265A adds a compensating ramp to the MOSFET switch current sense signal. This slope compensation prevents sub-harmonic oscillations at duty cycles greater than 50%. The peak current limit of the high side switch is not affected by the slope compensation and remains constant over the full duty cycle range

- **PULSE SKIP MODE**

The DP31265A operates in a pulse skipping mode at light load currents to improve efficiency by reducing switching and gate drive losses. If the output voltage is within regulation and the peak switch current at the end of any switching cycle is below the pulse skipping current threshold, the device enters pulse skipping mode. The pulse skipping current threshold is the peak switch current level corresponding to a nominal COMP voltage of 600mV. When in this mode, the COMP terminal voltage is clamped at 600mV and the high side MOSFET is inhibited. Since the device is not switching, the output voltage begins to decay. The voltage control loop responds to the falling output voltage by increasing the COMP terminal voltage. The high side MOSFET is enabled and switching resumes when the error amplifier lifts COMP above the pulse skipping threshold. The output voltage recovers to the regulated value,and COMP eventually falls below the mode pulse skipping threshold at which time the device again enters pulse skipping mode. The internal PLL remains operational when in pulse skipping mode. When operating at light load currents in pulse skipping mode, the switching transitions occur synchronously with the external clock signal

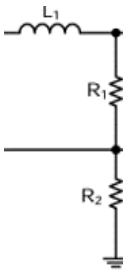
APPLICATION INFORMATION

The output stage of Asynchronous buck converter is mainly composed of inductor and capacitors. By switching the internally integrated High Side power MOSFET, the energy is stored and transferred to the load, and the second-order LC filter is formed to smooth the switching node voltage so that the stable output DC voltage is obtained.

- **Setting Output Voltage**

The output voltage is set by FB voltage, which is divided by resistor (R1 & R2) from output node to Ground. That resistor with 1% or higher accuracy is preferred. The output voltage value is set by equation as below.

$V_{OUT}=V_{FB} \times ((R1+R2)/R2)$



Vref is the internal reference voltage of DP31265A, 0.8V.

Table1 Recommend Component Selection Table

VOUT (V)	R1 (kΩ)	R2 (kΩ)	BS (uF)	D1	L1 (uH)	CIN (uF)	COUT (uF)
5	10.5	2	0.1	SS510	22	22	44
9	20.5	2	0.1	SS510	22	22	44
12	28	2	0.1	SS510	22	22	44

- **Inductor selection**

An inductor is required to supply constant current to the load while being driven by the switched input voltage. The common value of the inductance is between 22uH to 33uH. A larger value inductor will result in less current ripple and lower output voltage ripple. However, the larger value inductor will have larger physical size, higher DC resistance, and/or lower saturation current. A good rule to calculate the inductance is to allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum load current. At the same time, it is needed to make sure that the peak inductor current is below the inductor saturation current.

The inductance value can be calculated by:

$$L=\frac{V_{OUT}}{f_s \times \Delta I_L}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

Where VOUT is the output voltage, VIN is the input voltage, fs is the switching frequency, and ΔL is the peak-to-peak inductor ripple current.

The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

The choice of which style inductor to use mainly depends on the price vs. size requirements and any EMI constraints.

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency

- **Input capacitors selection**

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the converter. It is recommend to use low ESR capacitors to optimize the performance. Ceramic capacitor is preferred, but tantalum or low-ESR electrolytic capacitors may also meet the requirements. It is better to choose X5R or X7R dielectrics when using ceramic capacitors.

Since the input capacitor (CIN) absorbs the input switching current, a good ripple current rating is required for the capacitor. The RMS current in the input capacitor can be estimated by:

$$I_{CIN}=I_{load} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1-\frac{V_{OUT}}{V_{IN}}\right)}$$

The worst-case condition occurs at VIN = 2×VOUT, where:

$$I_{CIN}=\frac{I_{load}}{2}$$

For simplification, choose the input capacitor whose RMS current rating is greater than half of the maximum load current. When electrolytic or tantalum capacitors are used, a small, high quality ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible. When ceramic capacitors are used, make sure that they have enough capacitance to maintain voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN}=\frac{I_{load}}{f_s\times C_{IN}}\times\frac{V_{OUT}}{V_{IN}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

CIN is the input capacitance.

- **Output capacitors selection**

The output capacitor (COUT) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT}=\frac{V_{OUT}}{f_s\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times\left(R_{ESR}+\frac{1}{8\times f_s\times C_{OUT}}\right)$$

Where L is the inductor value, RESR is the equivalent series resistance (ESR) value of the output capacitor and COUT is the output capacitance value. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly determined by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT}=\frac{V_{OUT}}{8\times f_s^{2}\times L\times C_{OUT}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT}=\frac{V_{OUT}}{f_s\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The DP31212S/FS can be optimized for a wide range of capacitance and ESR values.

- **Bootstrap Capacitor Selection**

The recommended capacitor is 0.1 μF and rated 16 V or higher. The bootstrap capacitor is located between the SW pin and the BOOT pin. The bootstrap capacitor must be a high-quality ceramic type with an X7R or X5R grade dielectric for temperature stability.

- **Schottky Diode Selection**

The breakdown voltage rating of the diode is preferred to be 25% higher than the maximum input voltage. The current rating for the diode must be equal to the maximum output current for best reliability in most applications. In cases where the input voltage is much greater than the output voltage, the average diode current is lower. In this case it is possible to use a diode with a lower average current rating, approximately (1-D) × IOUT however the peak current rating must be higher than the maximum load current. A 3-A rated diode is a good starting point.

- **PCB Layout**

PCB layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion efficiency, thermal performance, and minimized EMI.

1. The feedback network, resistor R13 and R14, should be kept close to FB pin. Vout sense path should stay away from noisy nodes, such as SW & BS signals and preferably through a layer on the other side of shielding layer.

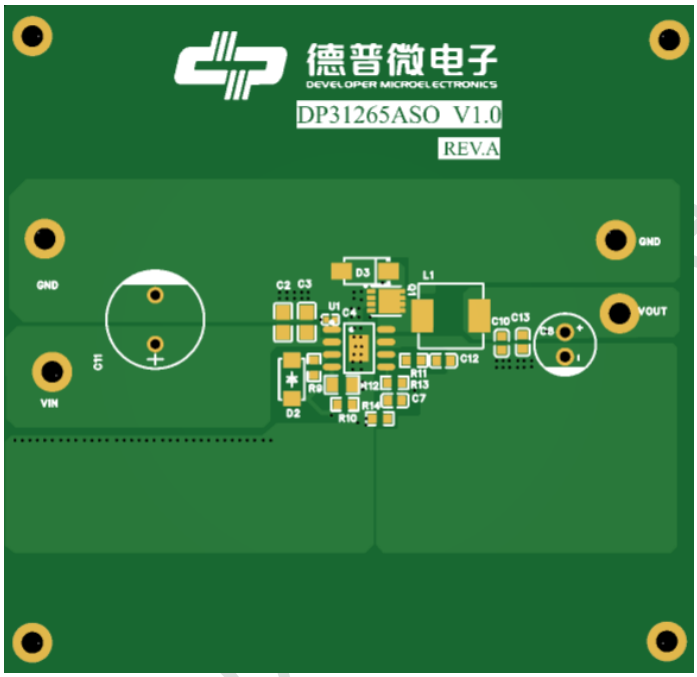
2. The input bypass capacitor C3 and C2 must be placed as close as possible to the VIN pin and ground. Grounding for both the input and output capacitors should consist of localized top side planes that connect to the GND pin and PAD. It is a good practice to place a ceramic cap near the VIN pin to reduce the high frequency injection current.

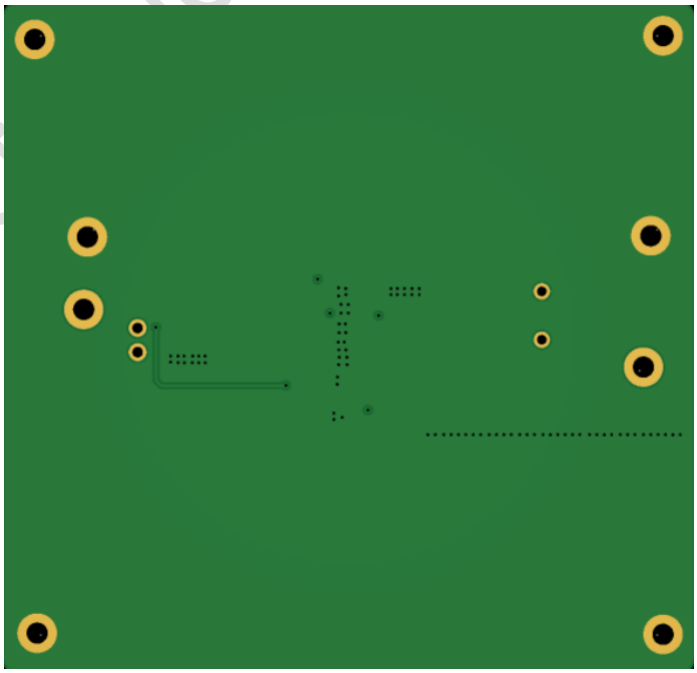
3. The inductor L should be placed close to the SW pin to reduce magnetic and electrostatic noise.

4. The output capacitor, COUT should be placed close to the junction of L and the diode D. The L, D, and COUT trace should be as short as possible to reduce conducted and radiated noise and increase overall efficiency.

5. The ground connection for C3, C2,C11 and C8, C10 ,C13 should be as small as possible and connect to system ground plane at only one spot (preferably at the COUT ground point) to minimize injecting noise into system ground plane.

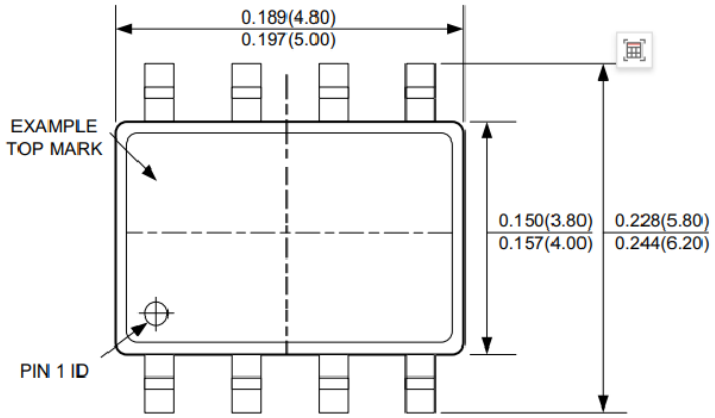
6. Large GND Copper Pour near IC is recommended to minimize the heat of IC.



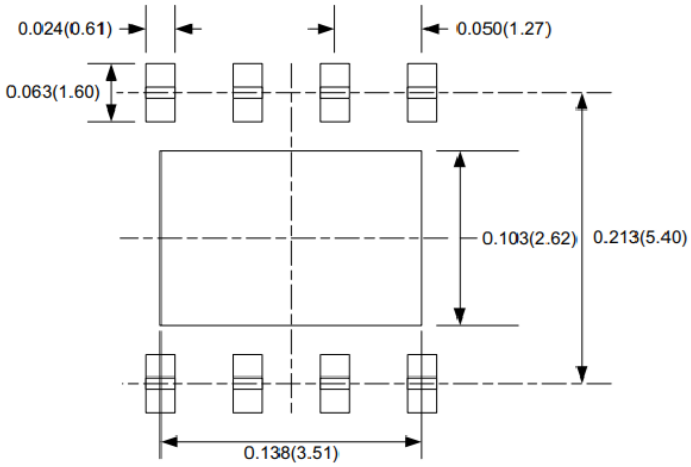


PACKAGE DIMENSION

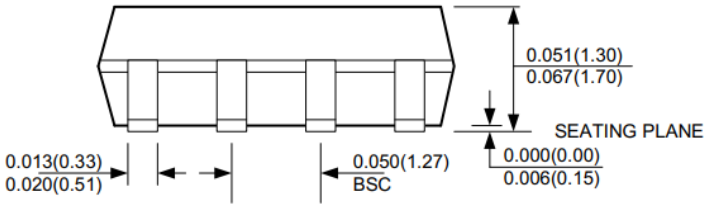
ESOP8 (EXPOSED PAD)



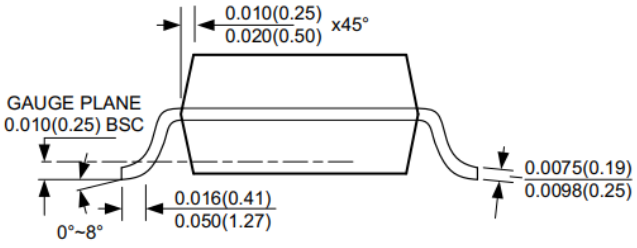
TOP VIEW



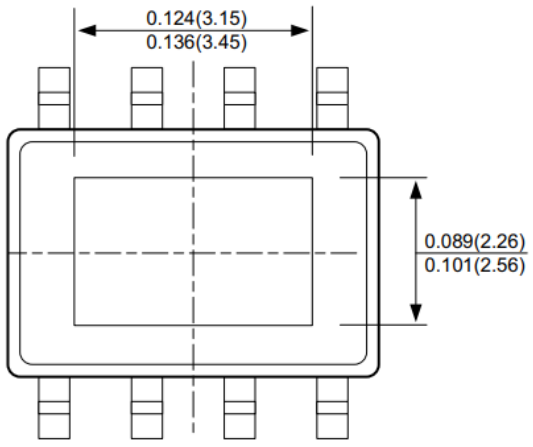
RECOMMENDED PAD LAYOUT



FRONT VIEW



SIDE VIEW



BOTTOM VIEW

NOTE:
1. CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2. PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5. DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6. DRAWING IS NOT TO SCALE.

REVISION HISTORY

Editions	Revised Date	Redaction person	Revision content
A.0	2023/12/23	PXB	First release

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