

5V to 100V Input, 1A Asyn. Low IQ Buck Converter

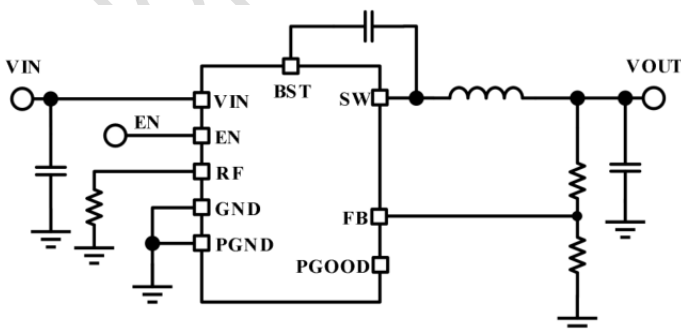
FEATURES

- Input Voltage Range: 5V to 100V
- Peak and valley current limit protection
- Continuous Output Current: 1A
- Adjustable switching frequency to 2MHZ
- Reference Voltage: 1.2V \pm 1.5% @25°C
- Integrated high side 0.7 Ω NFET and low side 0.34 Ω NFET switch supports wide duty cycle range
- Low Quiescent Current: 25 μ A
- Low Shutdown Current: 2.5 μ A
- EN UVLO and thermal shutdown protection
- Optional Operation Modes at Light-Load
- Internal VCC bias regulator and boot diode
- Over Current Protection
- Fixed 3ms Internal soft start timer
- Short Protection with Hiccup-Mode
- Thermal Shutdown Protection
- Open drain power good indicator
- ESOP8 package

APPLICATIONS

- High-cell-count battery packs (E-Bike, E-Scooter)
- POE
- Appliances, power and garden tools
- Motor drives, drones, telecom
- Industrial Automation and Motor Control
- USB Dedicated Charging Ports and Battery Chargers
- Vehicle Accessories: GPS, Entertainment

TYPICAL APPLICATION CIRCUIT



DESCRIPTIONS

The DP312101ASO asynchronous buck converter is designed to regulate over a wide input voltage range, minimizing the need for external surge suppression components. A minimum controllable on time of 100ns facilitates large step down conversion ratios, enabling the direct step down from a 48V nominal input to low-voltage rails for reduced system complexity and solution cost. The DP312101ASO operates during input voltage dips as low as 5V, at nearly 100% duty cycle if needed, making it an excellent choice for wide input supply range industrial and high cell count battery pack applications.

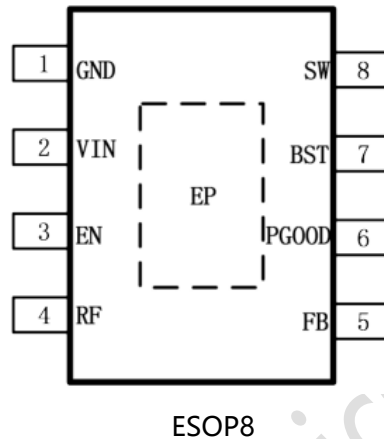
With integrated high side power MOSFET, the DP312101ASO delivers up to 1A of output current. A constant on time (COT) control architecture provides nearly constant switching frequency with excellent load and line transient response. Additional features of the DP312101ASO include ultra low IQ and high light load efficiency, innovative peak and valley over current protection, integrated VCC bias supply and bootstrap diode, precision enable and input UVLO, and thermal shutdown protection with automatic recovery.

ORDERING INFORMATION

Part Number	Description
ESOP8	Pb free in T&R, 4000 Pcs/Reel

PRODUCT DESCRIPTION

➤ Pin Arrangement

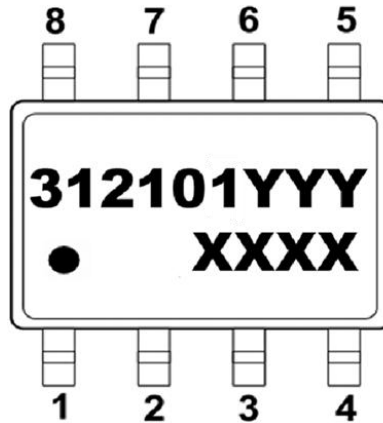


➤ Pin Configuration

ESOP8	Pin Name	Description
1	GND	Ground Pin
2	VIN	Regulator supply input pin to high side power MOSFET and internal bias regulator. Connect directly to the input supply of the buck converter with short, low impedance paths.
3	EN/UVLO	Precision enable and under voltage lockout (UVLO) programming pin. If the EN/UVLO voltage is below 1.1V, the converter is in the shutdown mode with all functions disabled. If the UVLO voltage is greater than 1.1V and below 1.5V, the converter is in standby mode with the internal VCC regulator operational and no switching. If the EN/UVLO voltage is above 1.5V, the start up sequence begins. This pin has an internal pull up 10M ohm resistor to make sure IC work when EN pin is float.
4	RF	On time programming pin. A resistor between this pin and GND sets the buck switch on Time.
5	FB	Feedback input of voltage regulation comparator.
6	PGOOD	Power good indicator. This pin is an open drain output pin. Connect to a source voltage through an external pull up resistor between 10kΩ to 100kΩ
7	BST	Supply input for the high-side NFET gate drive circuit. Connect a 0.1μF capacitor between VBST and SW pins.
8	SW	Switching node that is internally connected to the source of the high side NMOS buck switch and the drain of the low side NMOS synchronous rectifier. Connect to the switching node of the power inductor.

9	EP	Exposed pad of the package. No internal electrical connection. Solder the EP to the GND pin and connect to a large copper plane to reduce thermal resistance.
---	----	---

➤ Marking Information



DP312101 for product name:

YYY refers to the following table description, represents different packaging and special functions

XXXX The first X represents the last year, 2020 is 0; The second X represents the month, in A-L 12 letters; The third and fourth X on behalf of the date, 01-31 said;

Marking	Model	Description
312101A	DP312101ASO	DP312101ASO Buck Converter, 5V~100V, 1A, VFB 1.2V, ESOP8

➤ Absolute Maximum Ratings

PARAMETER	Min	Max	Unit
VIN Voltage	-0.3	100	V
EN Voltage	-0.3	100	V
SW Voltage(DC)	-0.3	100	V
SW Voltage(AC less than 10ns while Switching)	-1.5	100	V
FB Voltage	-0.3	5.5	V
PG Voltage	-0.3	100	V
BS Voltage(vs SW)	-0.3	5.5	V
Operating junction temperature,TJ	-40	150	°C
Storage temperature, Tstg	-65	150	°C
Lead Temperature (Soldering, 10sec.)	-	260	°C

Over operating temperature range (unless otherwise noted)(1)

Note:(1)Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal

➤ Recommended Operating Conditions

PARAMETER	Min	Max	Unit
VIN Voltage(VIN)	5	100	V
Output current	0	1	A
TJ	-40	125	°C

Note : (1)All limits specified at room temperature (TA = 25°C) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

ESD Ratings

PARAMETER	Description	Value	Unit
HBM	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
CDM	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±200	V

Note : (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

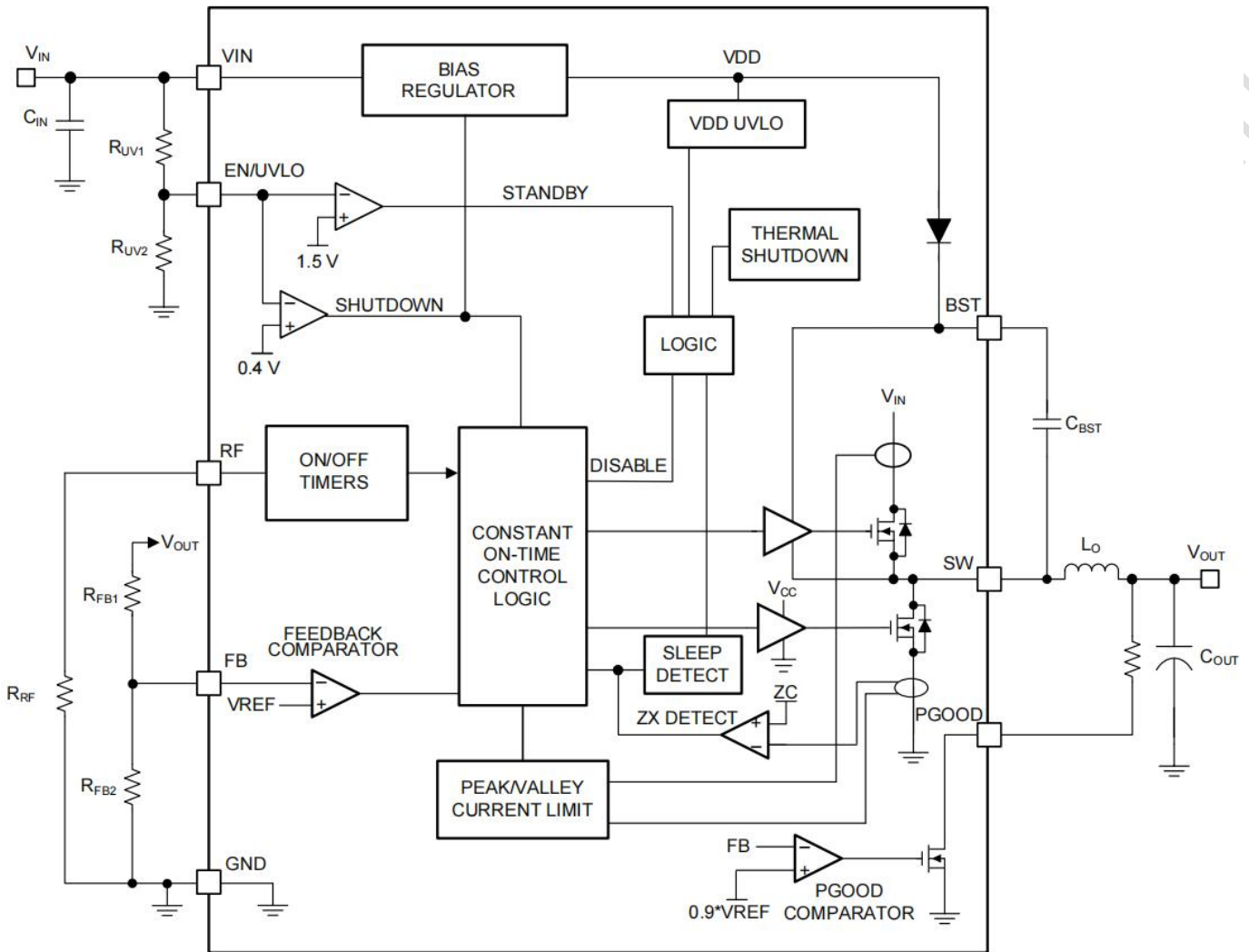
➤ Thermal Information

THERMAL METRIC	Description	ESOP8	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽¹⁾⁽²⁾	41.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.3	°C/W
$R_{\theta JB}$	Junction-to-board(Bottom) thermal resistance	25.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	8.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	25.2	°C/W

Note (1): The package thermal impedance is calculated in accordance to JESD 51-7.

Note (2): Thermal Resistances were simulated on a 4-layer, JEDEC board

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

(Typical at $V_{in}=24V$, $V_{EN}=2V$, $T_J=25^{\circ}C$, unless otherwise noted.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input Voltage	V_{IN}		5		100	V
V_{IN} Quiescent Current	I_Q	$V_{EN}=2.5V$		25	50	μA
Shutdown Current	I_{SHDN}	$V_{EN}=0V$		2.5	5	μA
FB Voltage	V_{FB}	$T_J=25^{\circ}C$	1.18	1.2	1.218	V
Switching Frequency	F_{SW}	$R_{RF}=500 K\Omega$		200		KHZ
		$R_{RF}=330K\Omega$		300		KHZ
		$R_{RF}=200K\Omega$		500		KHZ
Current Limit Threshold	$I_{HS}(OC)$		1.2			A
High-Side MOS ON-Resistance	$R_{DSON}(HS)$			700		m Ω
Low-Side MOS ON-Resistance	$R_{DSON}(LS)$			340		m Ω
EN Rising Threshold	$V_{EN}(R)$	EN Rising	1.45	1.5	1.55	V
EN Falling Threshold	$V_{EN}(F)$	EN Falling	1.35	1.4	1.44	V
FB upper threshold for PGOOD high to low	V_{PG-UTH}		1.105	1.14	1.175	V
FB lower threshold for PGOOD high to low	V_{PG-LTH}		1.055	1.08	1.1	V
PGOOD upper and lower threshold hysteresis	V_{PG-HYS}			60		mV
PGOOD pull down resistance	R_{PG}			200		Ω
VSD-Rising	VSD-Rising	EN Rising			1.1	V
VSD-Falling	VSD-Falling	EN Falling	0.45			V
Gate Driver UVLO	V_{bst-UV}	V_{bst} Rising		2.7	3.4	V
Soft Start	T_{SS}	10%* V_{out} to 90%* V_{out}		3		ms
Over-Temperature Protection	T_{SD}			175		$^{\circ}C$
Over-Temperature Protection hysteresis	ΔT_{SD}			10		$^{\circ}C$

TYPICAL CHARACTERISTICS

Test Condition: TA = 25°C, VIN=48V, Vout=12V, unless otherwise noted.

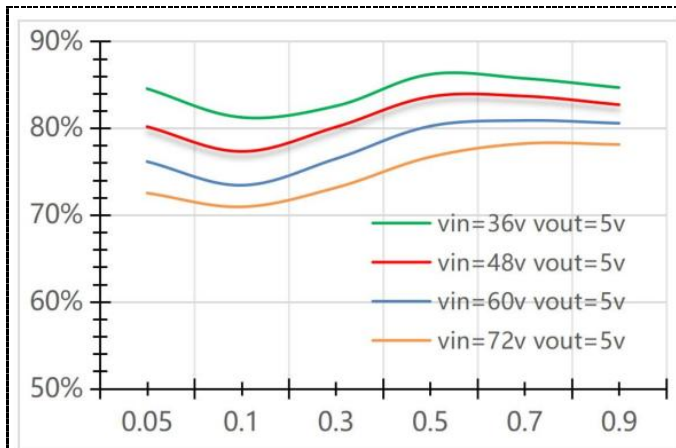


Figure1 5V Output Efficiency

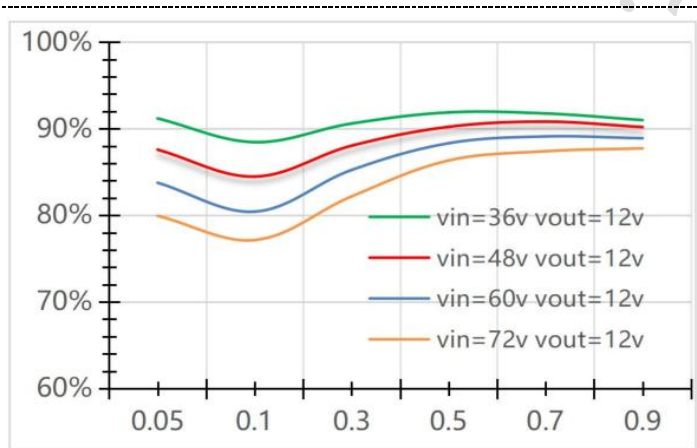


Figure2 12V Output Efficiency

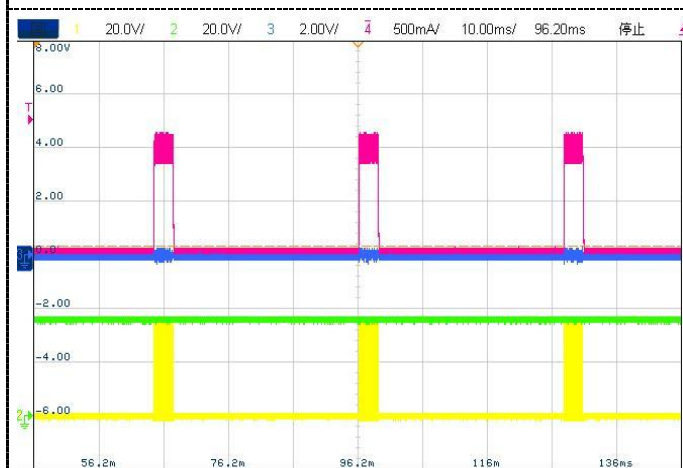


Figure3 Vin=36V Vout=12V Short Circuit waveform

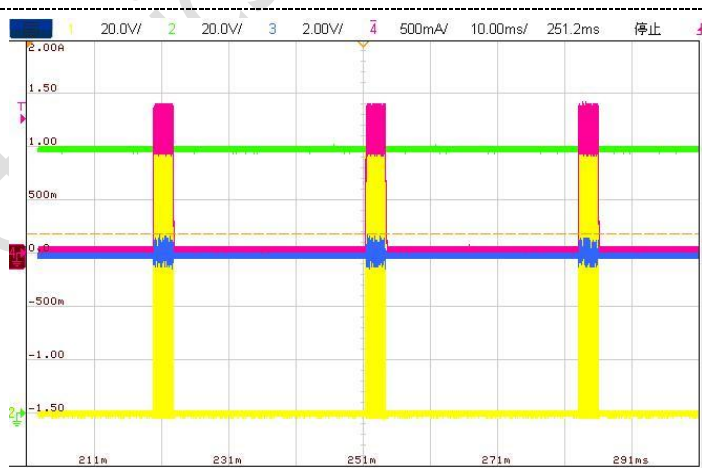
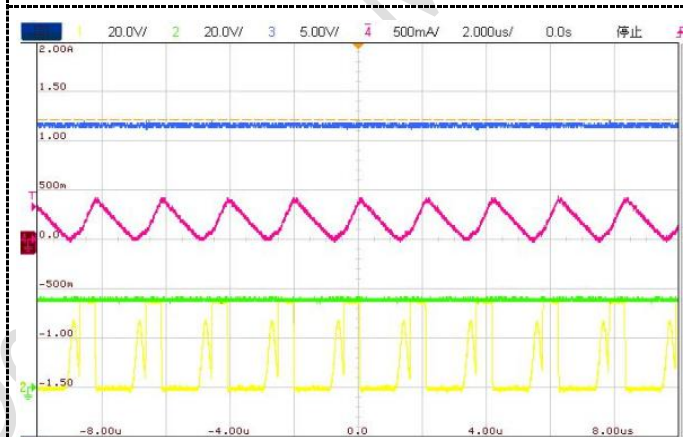


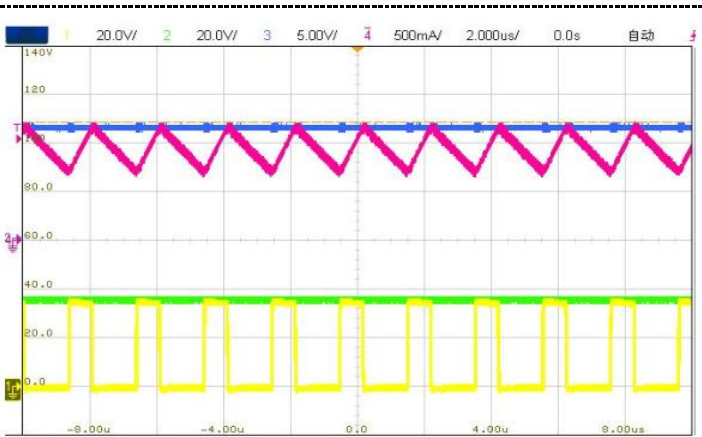
Figure4 Vin=100V Vout=12V Short Circuit waveform



绿色: Vin 黄色: SW 蓝色: Vout 红色: IL

Vin=36V Vout=12V

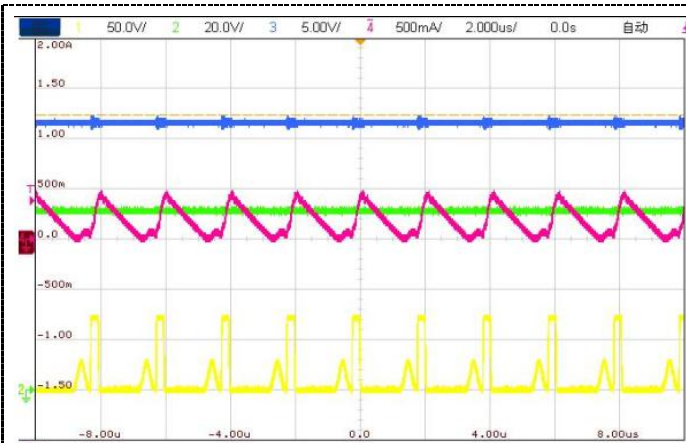
Figure5 DCM with Iout=0.15A



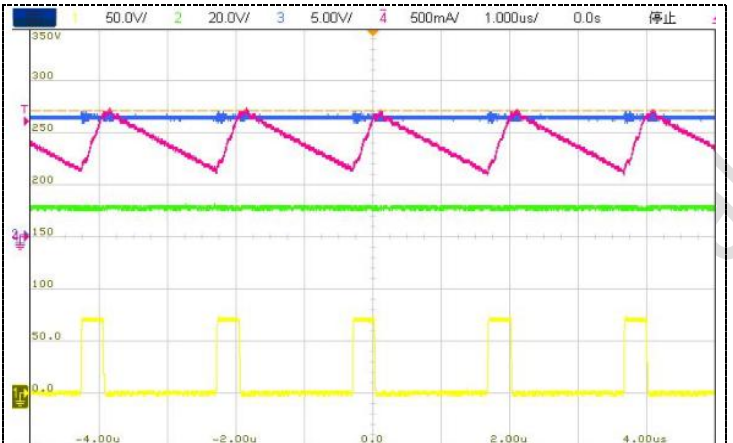
绿色: Vin 黄色: SW 蓝色: Vout 红色: IL

Vin=36V Vout=12V

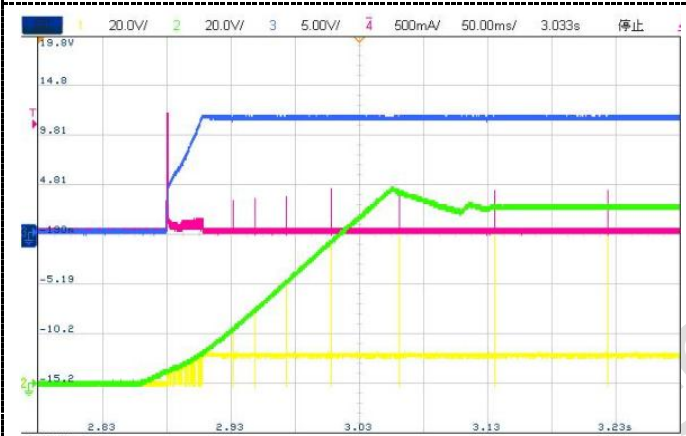
Figure6 DCM with Iout=0.9A



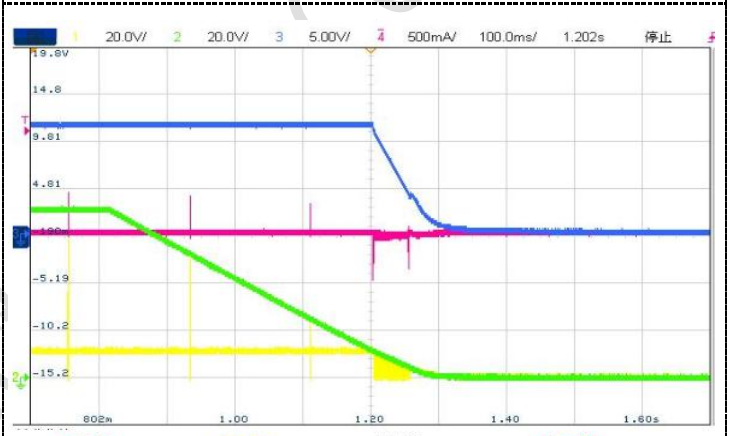
绿色: Vin 黄色: SW 蓝色: Vout 红色: IL
Vin=72V Vout=12V
Figure7 DCM with Iout=0.16A



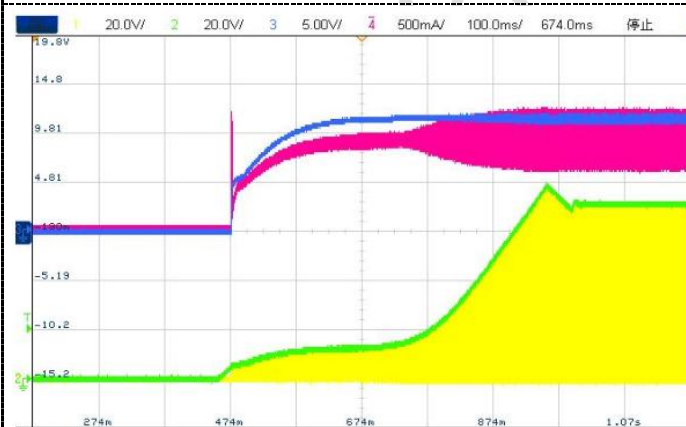
绿色: Vin 黄色: SW 蓝色: Vout 红色: IL
Vin=72V Vout=12V
Figure8 CCM with Iout=0.9A



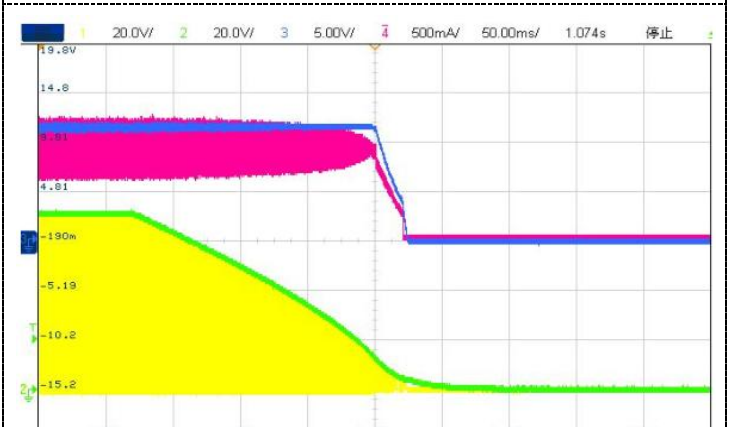
绿色: Vin 黄色: SW 蓝色: Vout 红色: IL
Vin=72V Vout=12V
Figure9 VIN StartUp with No Load



绿色: Vin 黄色: SW 蓝色: Vout 红色: IL
Vin=72V Vout=12V
Figure10 ShutDown with No Load



绿色: Vin 黄色: SW 蓝色: Vout 红色: IL
Vin=72V Vout=12V
Figure11 VIN StartUp with 0.9A Load



绿色: Vin 黄色: SW 蓝色: Vout 红色: IL
Vin=72V Vout=12V
Figure12 VIN ShutDown with 0.9A Load

➤ Control Architecture

The DP312101ASO step down switching converter employs a constant on time (COT) control scheme. The COT control scheme sets a fixed on time t_{ON} of the high side FET using a timing resistor (R_{ON}). The t_{ON} is adjusted as V_{in} changes and is inversely proportion to input voltage to maintain a fixed frequency when in continuous conduction mode (CCM). After expiration of t_{ON} , the high side FET remains off until the feedback pin is equal or below the reference voltage of 1.2V. In order to maintain stability, the feedback comparator requires a minimal ripple voltage that is in phase with the inductor current during the off time. Furthermore, this change in feedback voltage during the off time must be large enough to dominate any noise present at the feedback node. The minimum recommended ripple voltage is 20mV. Refer to Table for different types of ripple injection schemes that ensure stability over the full input voltage range. During a rapid start up or a positive load step, the regulator operates with minimum off times until regulation is achieved. This feature enables extremely fast load transient response with minimum output voltage undershoot. When regulating the output in steady state operation, the off time automatically adjusts itself to produce the SW pin duty cycle required for output voltage regulation to maintain a fixed switching frequency.

Ripple Generation Methods

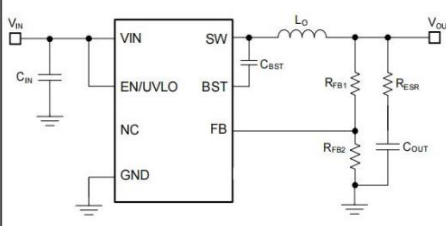
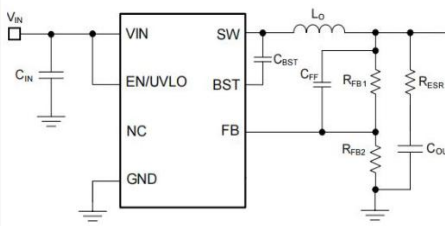
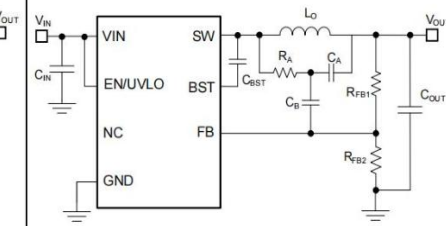
TYPE 1	TYPE 2	TYPE 3
Lowest Cost	Reduced Ripple	Minimum Ripple
		
$R_{ESR} \geq \frac{20\text{mV} \cdot V_{OUT}}{V_{FB1} \cdot \Delta I_{L(nom)}}$ $R_{ESR} \geq \frac{V_{OUT}}{2 \cdot V_{IN} \cdot F_{SW} \cdot C_{OUT}}$	$R_{ESR} \geq \frac{20\text{mV}}{\Delta I_{L(nom)}}$ $R_{ESR} \geq \frac{V_{OUT}}{2 \cdot V_{IN} \cdot F_{SW} \cdot C_{OUT}}$ $C_{FF} \geq \frac{1}{2\pi \cdot F_{SW} \cdot (R_{FB1} \parallel R_{FB2})}$	$C_A \geq \frac{10}{F_{SW} \cdot (R_{FB1} \parallel R_{FB2})} \quad (3)$ $R_A C_A \leq \frac{(V_{IN-nom} - V_{OUT}) \cdot t_{ON} (@V_{IN-nom})}{20\text{mV}} \quad (4)$ $C_B \geq \frac{t_{TR-settling}}{3 \cdot R_{FB1}} \quad (5)$ $C_B \geq \frac{t_{TR-settling}}{3 \cdot R_{FB1}} \quad (8)$

Table presents 3 different methods for generating appropriate voltage ripple at the feedback node. Type-1 ripple generation method uses a single resistor, R_{ESR} in series with the output capacitor. The generated voltage ripple has two components, capacitive ripple caused by the inductor ripple current charging and discharging the output capacitor and resistive ripple caused by the inductor ripple current flowing into the output capacitor and through series resistance R_{ESR} . The capacitive ripple component is out of phase with the inductor current and does not decrease monotonically during the off time. The resistive ripple component is in phase with the inductor current and decreases monotonically during the off time. The resistive ripple



must exceed the capacitive ripple at VOUT for stable operation. If this condition is not satisfied, unstable switching behavior is observed in COT converters, with multiple on time bursts in close succession followed by a long off time. **Equation 1** and **Equation 2** define the value of the series resistance RESR to ensure sufficient in phase ripple at the feedback node.

Type-2 ripple generation uses a CFF capacitor in addition to the series resistor. As the output voltage ripple is directly AC coupled by CFF to the feedback node, the RESR and ultimately the output voltage ripple are reduced by a factor of V_{OUT} / V_{FB1} .

Type-3 ripple generation uses an RC network consisting of RA and CA, and the switch node voltage to generate a triangular ramp that is in phase with the inductor current. This triangular wave is the AC coupled into the feedback node with capacitor CB. Because this circuit does not use output voltage ripple, it is suited for applications where low output voltage ripple is critical.

FUNCTIONS DESCRIPTION

Feature Description

The DP312101ASO is an easy to use, ultra low IQ constant on time (COT) asynchronous step down buck regulator. With integrated high side power MOSFET, the DP312101ASO is a low cost, highly efficient buck converter that operates from a wide input voltage of 5V to 100V, delivering up to 1A DC load current. The DP312101ASO is available in the ESOP8 package. This constant on time (COT) converter is ideal for low noise, high current, and fast load transient requirements, operating with a predictive on time switching pulse. Over the input voltage range, input voltage feed forward is employed to achieve a quasi fixed switching frequency. A controllable on time as low as 100ns permits high step down ratios and a minimum forced off time of 200ns provides extremely high duty cycles allowing VIN to drop close to VOUT before frequency fold back occurs. At light loads the device transitions into an ultra low IQ mode to maintain high efficiency and prevent draining battery cells connected to the input when the system is in standby. The DP312101ASO implements a smart peak and valley current limit detection circuit to ensure robust protection during output short circuit conditions. Control loop compensation is not required for this regulator, reducing design time and external component count. The DP312101ASO incorporates additional features for comprehensive system requirements, including an open drain Power Good circuit for power rail sequencing and fault reporting, internally fixed soft start, monotonic start up into prebiased loads, smart cycle by cycle current limit for optimal inductor sizing, and thermal shutdown with automatic recovery. These features enable a flexible and easy to use platform for a wide range of applications. The DP312101ASO supports a wide range of end equipment systems requiring a regulated output from a high input supply where the transient voltage deviates from its DC level. Examples of such end equipment systems are 48V automotive systems, high cell count battery pack systems, 24V industrial

systems, and 48V telecom and PoE voltage ranges. The pin arrangement is designed for a simple layout requiring only a few external components.

- **Power GOOD**

The DP312101ASO provides a PGOOD flag pin to indicate when the output voltage is within the regulation level. Use the PGOOD signal for start up sequencing of downstream converters or for fault protection and output monitoring. PGOOD is an open drain output that requires a pull up resistor to a DC supply. The typical range of pull up resistance is 10kΩ to 100kΩ. When the FB voltage exceeds 95% of the internal reference VREF, the internal PGOOD switch turns off and PGOOD can be pulled high by the external pull up. If the FB voltage falls below 90% of VREF, an internal 25Ω PGOOD switch turns on and PGOOD is pulled low to indicate that the output voltage is out of regulation. The rising edge of PGOOD has a built in deglitch delay of 5μs.

- **Internal VCC Regulator and Bootstrap Capacitor**

The DP312101ASO contains an internal linear regulator that is powered from VIN with a nominal output of 5V, eliminating the need for an external capacitor to stabilize the linear regulator. The internal VCC regulator supplies current to internal circuit blocks including FET driver and logic circuits. The input pin (VIN) can be connected directly to line voltages up to 100V. As the power MOSFET has a low total gate charge, use a low bootstrap capacitor value to reduce the stress on the internal regulator. It is required to select a high quality 10nF 50V X7R ceramic bootstrap capacitor as specified in the Absolute Maximum Ratings. Selecting a higher value capacitance stresses the internal VCC regulator and damages the device. A lower capacitance than required may not be sufficient to drive the internal gate of the power MOSFET. An internal diode connects from the linear regulator to the BST pin to replenish the charge in the high side

gate drive bootstrap capacitor when the SW voltage is low

- **Soft Start**

The DP312101ASO employs an internal soft start control ramp that allows the output voltage to gradually reach a steady state operating point, thereby reducing start up stresses and current surges. The soft start feature produces a controlled, monotonic output voltage start up. The soft start time is internally set to 3ms.

- **UNDER-VOLTAGE LOCKOUT (UVLO)**

The DP312101ASO contains a dual level EN/UVLO circuit. When the EN/UVLO voltage is below 1.1V (typical), the converter is in a low current shutdown mode and the input quiescent current (IQ) is dropped down to 5μA. When the voltage is greater than 1.1V but less than 1.5V (typical), the converter is in standby mode. In standby mode the internal bias regulator is active while the control circuit is disabled. When the voltage exceeds the rising threshold of 1.5V (typical), normal operation begins. Install a resistor divider from VIN to GND to set the minimum operating voltage of the regulator.

- **Adjustable Switching Frequency**

Determine the RRF resistor using Equation 2 to set a specific switching frequency in CCM.

$$F_{sw}(\text{kHz}) = \frac{100000}{RRF(\text{K}\Omega)} \quad (2)$$

- **Overvoltage Protection**

The DP312101ASO includes an internal junction temperature monitor to protect the device in the event of a higher than normal junction temperature. If the junction temperature exceeds 175°C (typical), thermal shutdown occurs to prevent further power dissipation and temperature rise. The DP312101ASO initiates a restart sequence when the junction temperature falls

to 165°C, based on a typical thermal shutdown hysteresis of 10°C. This is a nonlatching protection, and, as such, the device cycles into and out of thermal shutdown if the fault persists..

- **Thermal Protection**

The DP312101ASO includes an internal junction temperature monitor to protect the device in the event of a higher than normal junction temperature. If the junction temperature exceeds 175°C (typical), thermal shutdown occurs to prevent further power dissipation and temperature rise. The DP312101ASO initiates a restart sequence when the junction temperature falls to 165°C, based on a typical thermal shutdown hysteresis of 10°C. This is a nonlatching protection, and, as such, the device cycles into and out of thermal shutdown if the fault persists

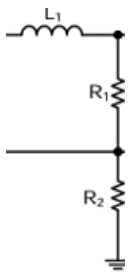
APPLICATION INFORMATION

The output stage of Asynchronous buck converter is mainly composed of inductor and capacitors. By switching the internally integrated High Side power MOSFET, the energy is stored and transferred to the load, and the second-order LC filter is formed to smooth the switching node voltage so that the stable output DC voltage is obtained.

● Setting Output Voltage

The output voltage is set by FB voltage, which is divided by resistor (R1 & R2) from output node to Ground. That resistor with 1% or higher accuracy is preferred. The output voltage value is set by equation as below.

$$V_{OUT} = V_{FB} \times ((R1 + R2)/R2)$$



Vref is the internal reference voltage of DP312101ASO, 1.2V.

Table1 Recommend Component Selection Table

VOUT (V)	R1 (kΩ)	R2 (kΩ)	BS (uF)	D1	L1 (uH)	CIN (uF)	COUT (uF)
5	31.6	10	0.1	SS5 10	33	22	44
12	91	10	0.1	SS5 10	33	22	44

● Inductor selection

An inductor is required to supply constant current to the load while being driven by the switched input voltage. The common value of the inductance is between 22uH to 33uH. A larger value inductor will result in less current ripple and lower output voltage

ripple. However, the larger value inductor will have larger physical size, higher DC resistance, and/or lower saturation current. A good rule to calculate the inductance is to allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum load current. At the same time, it is needed to make sure that the peak inductor current is below the inductor saturation current.

The inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_s \times \Delta I_L} \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

Where VOUT is the output voltage, VIN is the input voltage, fs is the switching frequency, and ΔL is the peak-to-peak inductor ripple current.

The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

The choice of which style inductor to use mainly depends on the price vs. size requirements and any EMI constraints.

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency

● Input capacitors selection

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the converter. It is recommend to use low ESR capacitors to optimize the performance. Ceramic capacitor is preferred, but tantalum or low-ESR electrolytic capacitors may also meet the requirements. It is better to choose X5R or X7R dielectrics when using ceramic capacitors.

Since the input capacitor (CIN) absorbs the input switching current, a good ripple current rating is required for the capacitor. The RMS current in the input capacitor can be estimated by:

$$I_{CIN} = I_{load} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}} \right)}$$

The worst-case condition occurs at VIN = 2×VOUT,

where:

$$I_{CIN} = \frac{I_{load}}{2}$$

For simplification, choose the input capacitor whose RMS current rating is greater than half of the maximum load current. When electrolytic or tantalum capacitors are used, a small, high quality ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible. When ceramic capacitors are used, make sure that they have enough capacitance to maintain voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{load}}{f_s \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

C_{IN} is the input capacitance.

- **Output capacitors selection**

The output capacitor (C_{OUT}) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_s \times C_{OUT}}\right)$$

Where L is the inductor value, RESR is the equivalent series resistance (ESR) value of the output capacitor and C_{OUT} is the output capacitance value. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly determined by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_s^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching

frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The DP31212S/FS can be optimized for a wide range of capacitance and ESR values.

- **Bootstrap Capacitor Selection**

The recommended capacitor is 0.1 μF and rated 16 V or higher. The bootstrap capacitor is located between the SW pin and the BOOT pin. The bootstrap capacitor must be a high-quality ceramic type with an X7R or X5R grade dielectric for temperature stability.

PCB LAYOUT

PCB layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion efficiency, thermal performance, and minimized EMI.

1. The feedback network, resistor R7 and R6, should be kept close to FB pin. Vout sense path should stay away from noisy nodes, such as SW & BS signals and preferably through a layer on the other side of shielding layer.
2. The input bypass capacitor C3 and C2 must be placed as close as possible to the VIN pin and ground. Grounding for both the input and output capacitors should consist of localized top side planes that connect to the GND pin and PAD. It is a good practice to place a ceramic cap near the VIN pin to reduce the high frequency injection

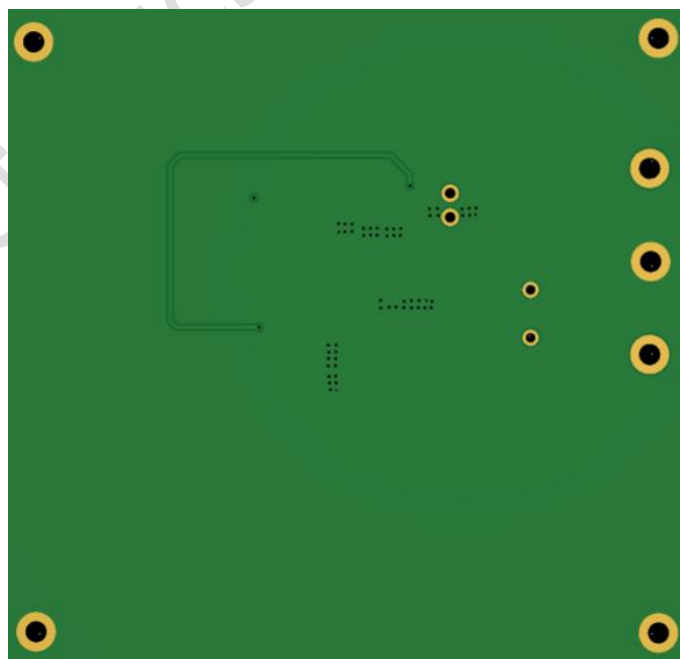
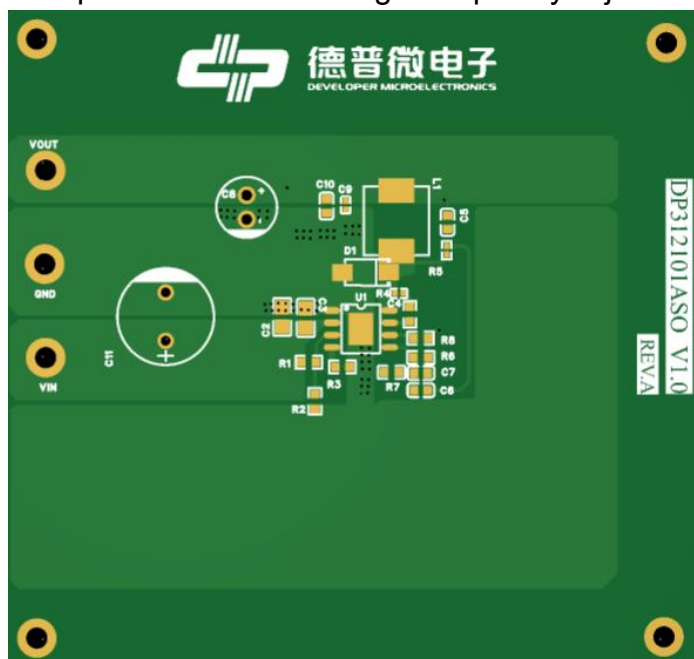
current.

3. The inductor L should be placed close to the SW pin to reduce magnetic and electrostatic noise.

4. The output capacitor, COUT should be placed close to the junction of L and the diode D. The L, D, and COUT trace should be as short as possible to reduce conducted and radiated noise and increase overall efficiency.

5. The ground connection for C3, C2, C11 and C8, C9, C10 should be as small as possible and connect to system ground plane at only one spot (preferably at the COUT ground point) to minimize injecting noise into system ground plane.

6. Large GND Copper Pour near IC is recommended to minimize the heat of IC.



APPLICATION Example

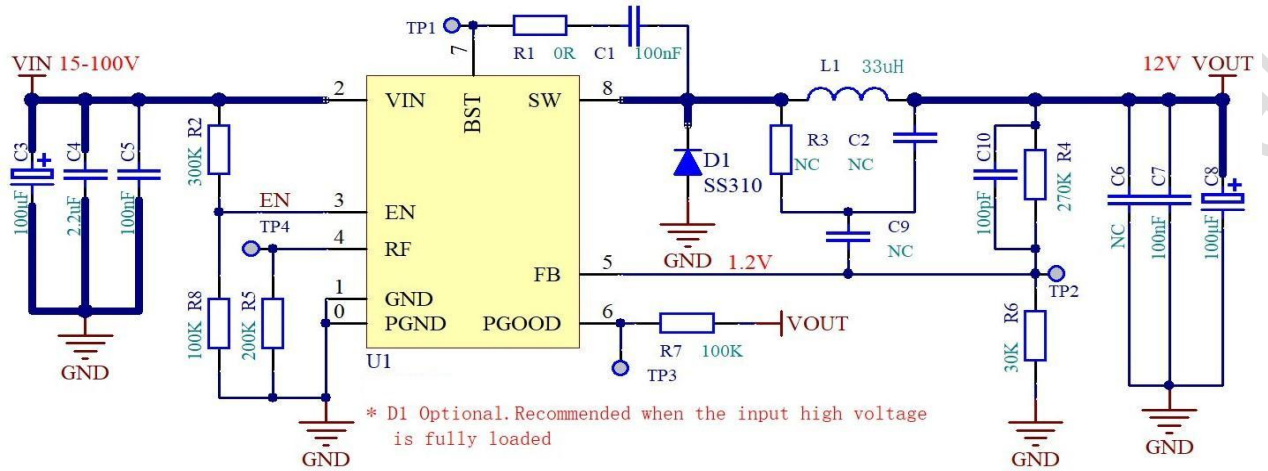
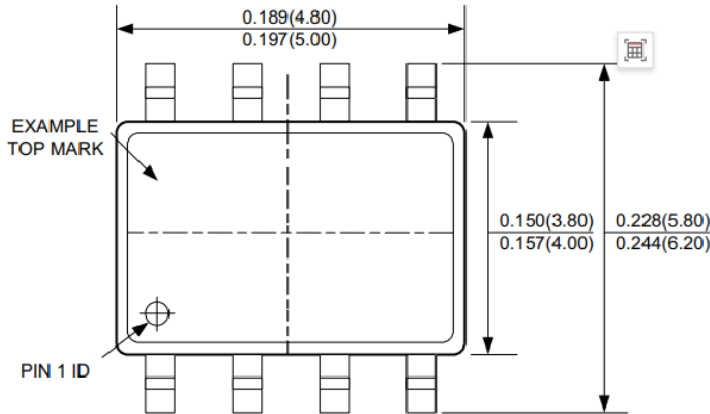


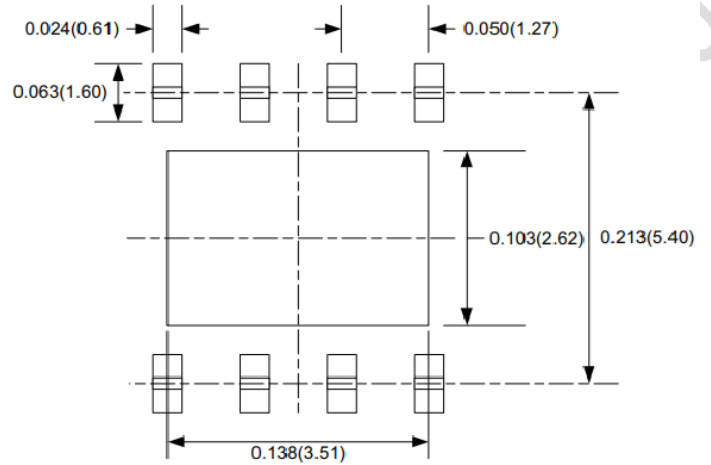
Fig. Schematic_1

PACKAGE DIMENSION

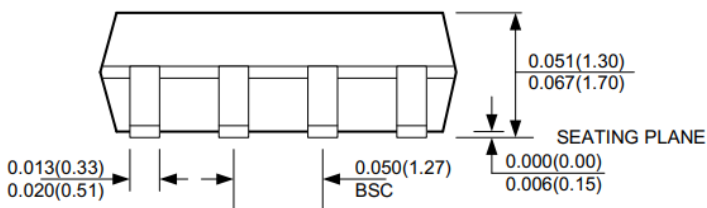
ESOP8 (EXPOSED PAD)



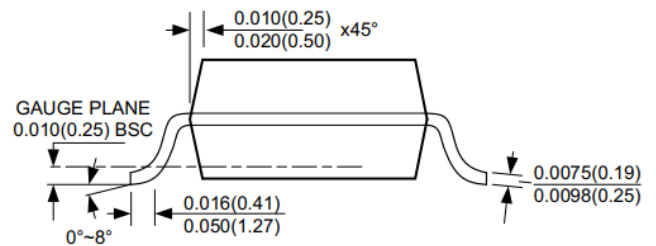
TOP VIEW



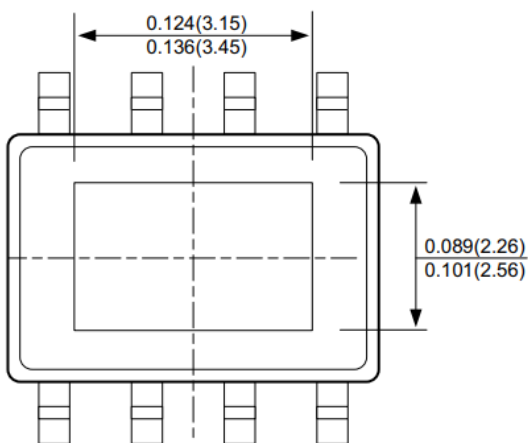
RECOMMENDED PAD LAYOUT



FRONT VIEW



SIDE VIEW



BOTTOM VIEW

NOTE:

- CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
- DRAWING IS NOT TO SCALE.



REVISION HISTORY

Editions	Revised Date	Redaction person	Revision content
A.0	2023/12/23	PXB	First release

Developer Microelectronics Confidential

OFFICIAL ANNOUNCEMENT

Division I will ensure the accuracy and reliability of the product specification document, but we reserve the right to independently modify the content of the specification document without prior notice to the customer. Before placing an order, customers should contact us to obtain the latest relevant information and verify that this information is complete and up-to-date. All product sales are subject to the sales terms and conditions provided by our company at the time of order confirmation.

Division I will periodically update the content of this document. Actual product parameters may vary due to differences in models or other factors. This document does not serve as any express or implied guarantee or authorization.

The product specification does not include any authorization for the intellectual property owned by our company or any third party. With respect to the information contained in this product specification, we make no explicit or implied warranties, including but not limited to the accuracy of the specification, its fitness for commercial use, suitability for specific purposes, or non-infringement of our company's or any third party's intellectual property. We also do not assume any responsibility for any incidental or consequential losses related to this specification document and its use.

We do not assume any obligations regarding application assistance or customer product design. Customers are responsible for their own use of our company's products and applications. In order to minimize risks associated with customer products and applications, customers should provide thorough design and operational safety validation.

The reproduction, transmission or use of this document or its contents is not permitted without express written authority. Once discovered, the company will pursue its legal responsibility according to law and compensate for all losses caused to the company.

Please note that the product is used within the conditions described in this document, paying particular attention to the absolute maximum rating, operating voltage range, and electrical characteristics. The Company shall not be liable for any damage caused by malfunctions, accidents, etc. caused by the use of the product outside the conditions stated in this document.

Division I has been committed to improving the quality and reliability of products, but all semiconductor products have a certain probability of failure, which may lead to some personal accidents, fire accidents, etc. When designing products, pay full attention to redundancy design and adopt safety indicators, so as to avoid accidents.

When using our chips to produce products, Division I shall not be liable for any patent dispute arising from the use of the chip in the product, the specification of the product, or the country of import, etc., in the event of a patent dispute over the products including the chip.