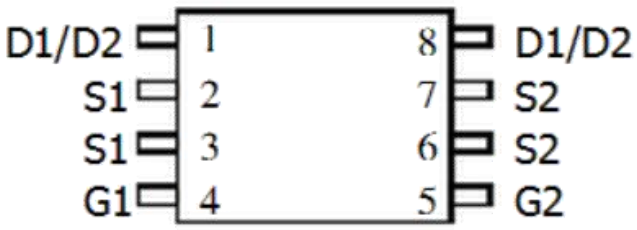
GENERAL DESCRIPTION

DP8206 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

PRODUCT SUMMARY

V_{DS}	20 V
I_D (at V_{GS}=4.5V)	10A
$R_{DS(ON)}$ (at V_{GS} = 4.5V)	7.1mΩ
$R_{DS(ON)}$ (at V_{GS} = 4.0V)	7.3mΩ
$R_{DS(ON)}$ (at V_{GS} = 3.8V)	7.4mΩ
$R_{DS(ON)}$ (at V_{GS} = 2.5V)	8.5mΩ

ESD Protected



Top View

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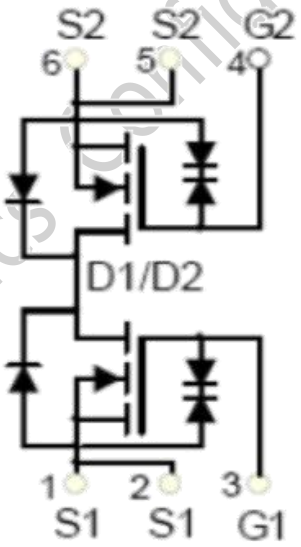


ABSOLUTE MAXIMUM RATINGS (TA=25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±10	V
Continuous Drain Current [c]	T_A=25℃	I_D	10	A
Pulsed Drain Current [a c]		I_{DM}	50	A
Junction and Storage Temperature Range		T_J,T_{STG}	-55 To 150	℃
Lead Temperature for Soldering Purposes(1/8' ' from case for 10 s)		TL	260	℃

THERMAL CHARACTERISTIC

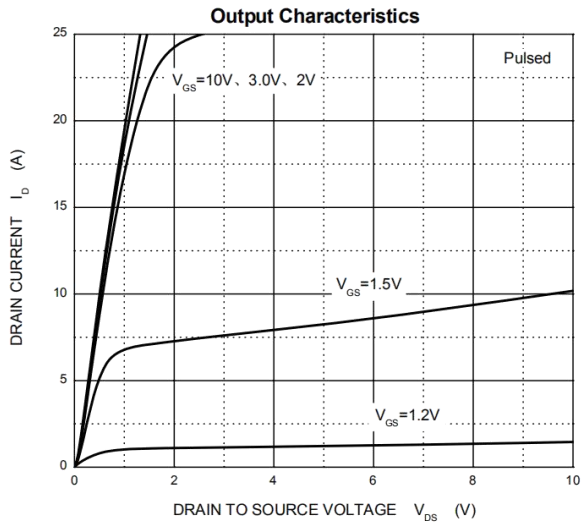
Parameter		Symbol	Limit	Unit
Maximum Junction-to-Ambient	Steady-State	$R_{\theta JA}$	83	℃/W

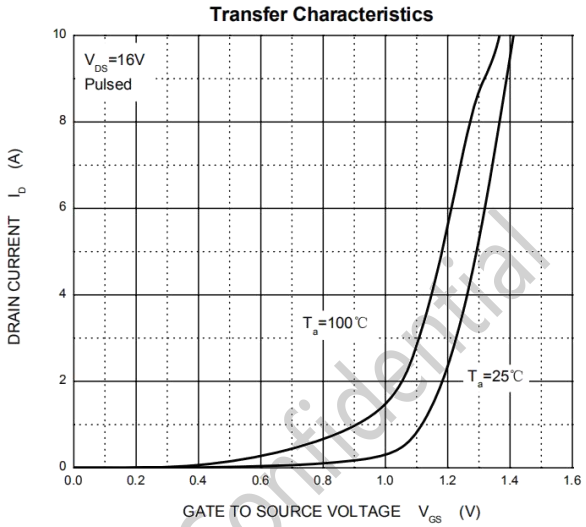
ELECTRICAL CHARACTERISTICS (TA=25℃ unless otherwise noted)

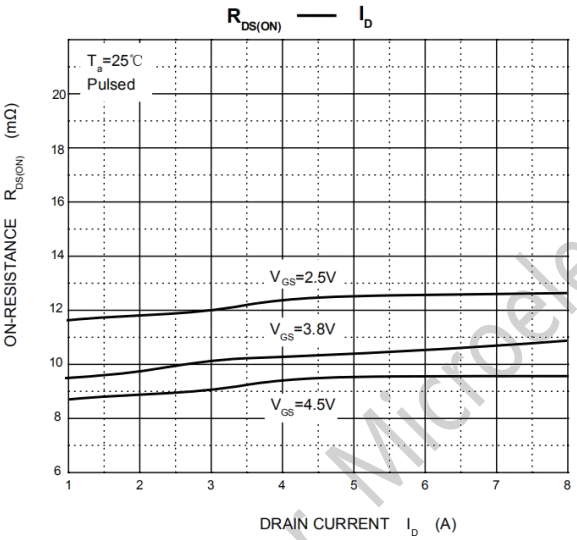
Parameter	Symbol	Condition	Min	Typc	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=250μA	20	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=20V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±10V,V_{DS}=0V	-	-	±10	μA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	0.5	-	1	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=4.5V, I_D=5A	-	7.1	9	mΩ
		V_{GS}=4V, I_D=5A	-	7.3	9.8	mΩ
		V_{GS}=3.8V, I_D=5A	-	7.4	10	mΩ
		V_{GS}=2.5V, I_D=5A	-	8.5	12	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=7A	9	36	-	S
Dynamic Characteristics [b]						
Input Capacitance	C_{lss}	V_{DS}=10V, V_{GS}=0V, F=1.0MHz	-	1950	-	pF
Output Capacitance	C_{oss}		-	250	-	pF
Reverse Transfer Capacitance	C_{rss}		-	210	-	pF
Switching Characteristics [b]						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=10V, V_{GS}=5V, RL=1.35Ω, R_{GEN}=3Ω,	-	2.2	-	nS
Turn-on Rise Time	t_r		-	5.9	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	40	-	nS
Turn-Off Fall Time	t_f		-	90	-	nS
Total Gate Charge	Q_g	V_{DS}=10V, I_D=4.5A, V_{GS}=7V	-	17	-	nC
Gate-Source Charge	Q_{gs}		-	2.0	-	nC
Gate-Drain Charge	Q_{gd}		-	5.1	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	V_{GS}=0V,I_S=1A	-	-	1	V
Maximum Body-Diode Continuous	I_S	-	-	-	6.0	A

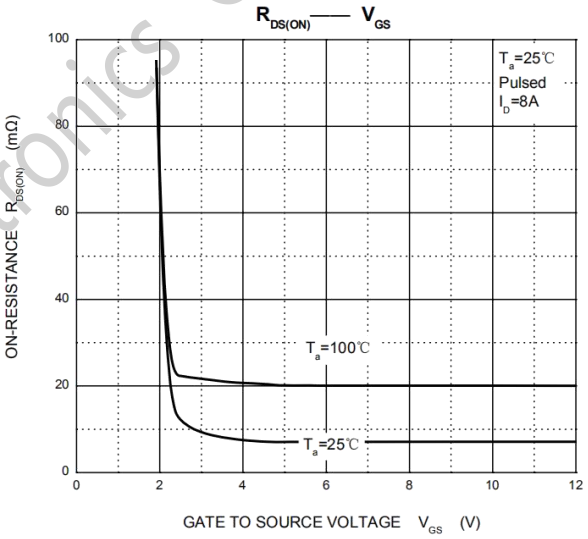
Notes
a.Pulse Test:Pulse Width < 300us, Duty Cycle < 0.5%.
b.Guaranteed by design, not subject to production testing.

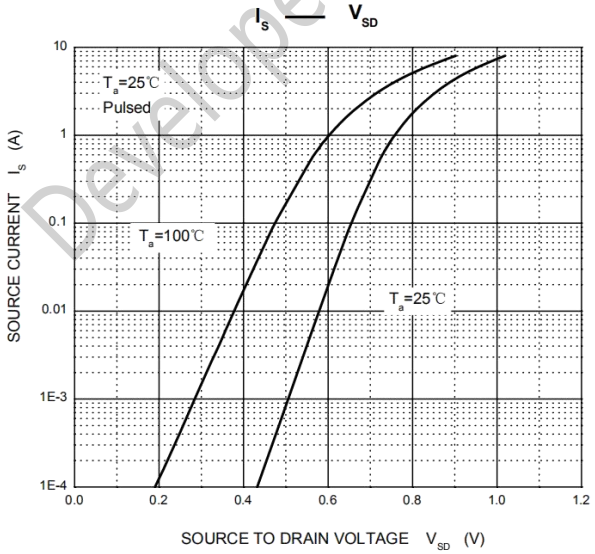
TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

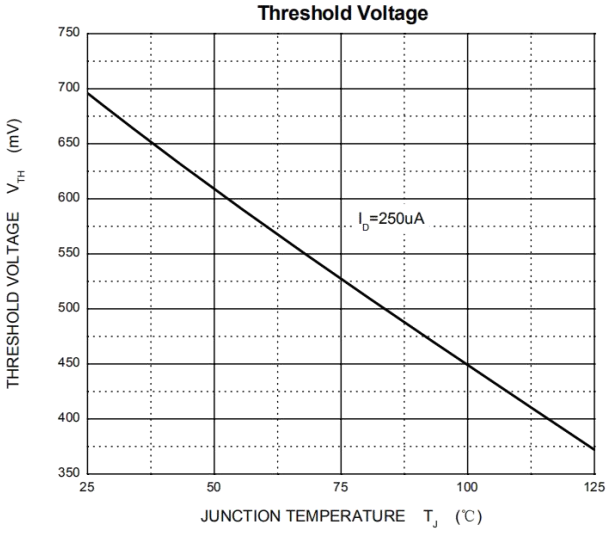


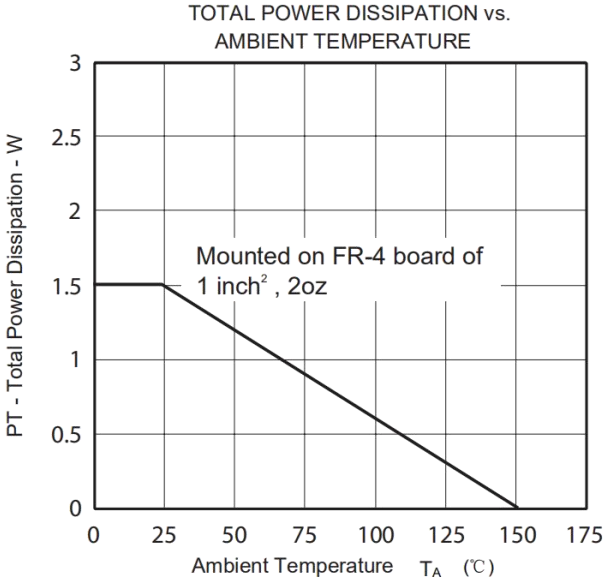


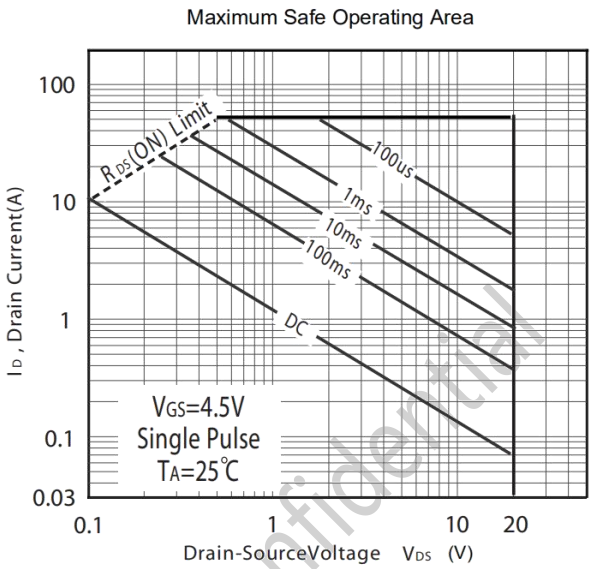


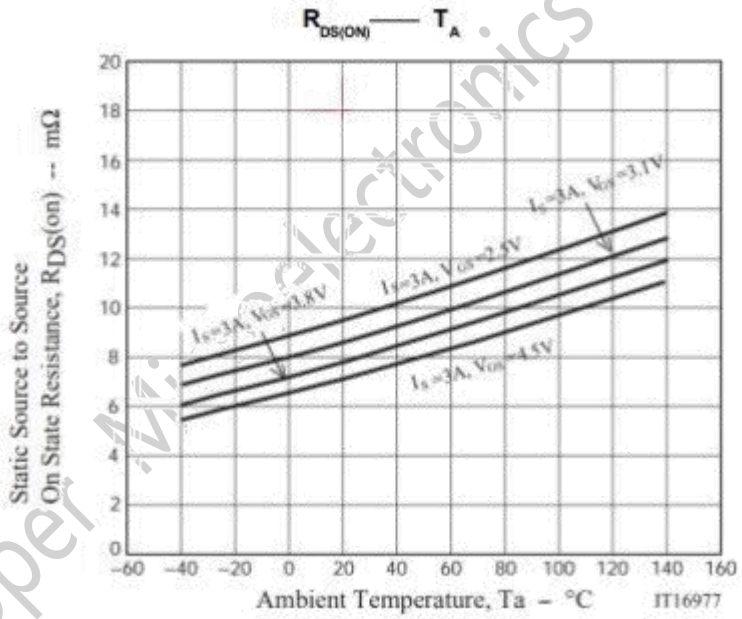












MARKING DESCRIPSION

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NOTE:

Y —Code of productive year code(the last number of the year)

M —Code of productive month(for example: A means January, B means February…)

DD —Productive date(the number of the date)

NN —Lot number of wafer

FOR EXCAMPLE:

5G1103

Means this product was produced in 2015-07-11 , and 03 is the wafer lot.

PACKAGE

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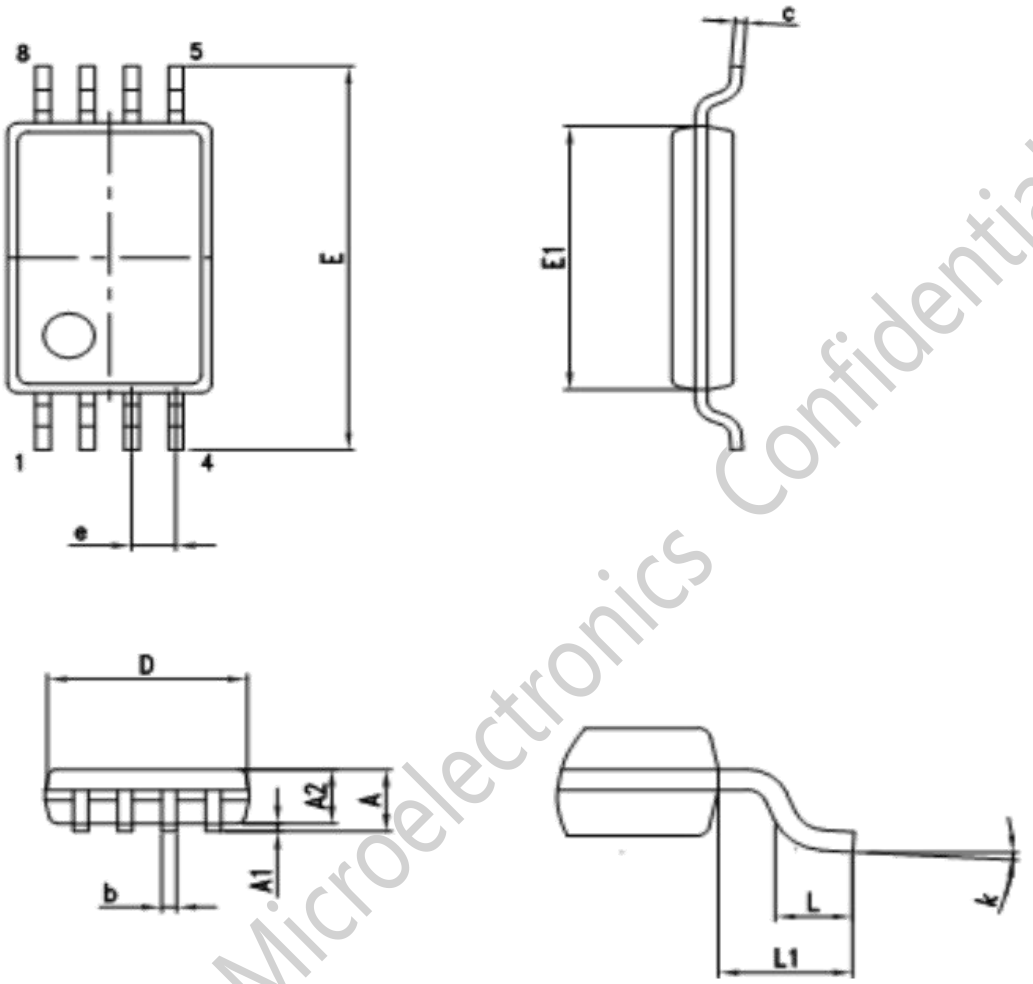

DIM.	mm.			inch.		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.05		1.20	0.041		0.047
A1	0.05		0.15	0.002		0.006
A2	0.80		1.05	0.032		0.041
b	0.19		0.30	0.008		0.012
c	0.090		0.20	0.003		0.007
D	2.90		3.10	0.114		0.122
E	6.20		6.60	0.240		0.260
E1	4.30		4.50	0.170		0.177
e		0.65			0.025	
L	0.45		0.75	0.018		0.030
L1		1.00			0.039	
k	0°		8°	0.192		0.208

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