GENERAL DESCRIPTION

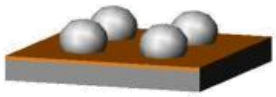
The DP8202 is Dual N-Channel enhancement MOS Field Effect Transistor and connecting the Drains on the circuit board is not required because the Drains of the MOSFET1 and the MOSFET2 are internally connected. Uses advanced trench technology and design to provide excellent RSS(ON) with low gate charge. This device is designed for Lithium-Ion battery protection circuit. The DP8202 is available in CSP 4L package. Standard Product DP8202 is Pb-free .

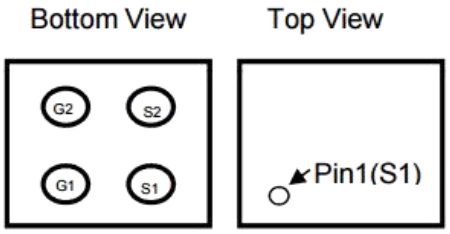
PRODUCT SUMMARY

Vss	12 V
I_S(at V_{GS}=4.5V)	6.0A
$R_{SS(ON)}$ (at V_{GS} = 4.5V)	<17mΩ
$R_{SS(ON)}$ (at V_{GS} = 4.0V)	<18mΩ
$R_{SS(ON)}$ (at V_{GS} = 3.1V)	<20mΩ
$R_{SS(ON)}$ (at V_{GS} = 2.5V)	<25mΩ

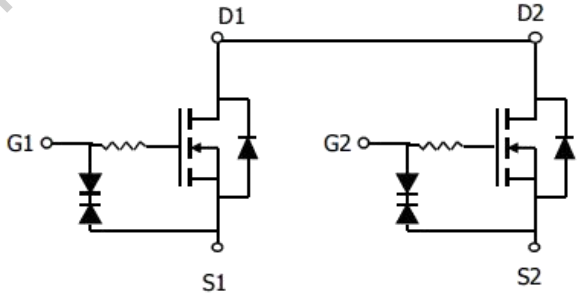
ESD Rating:2000V HBM

CSP 4L





Equivalent Circuit



ABSOLUTE MAXIMUM RATINGS TA=25°C unless otherwise noted

Parameter	Symbol	Limit	Unit
Source -Source Voltage	V_{SS}	12	V
Gate-Source Voltage	V_{GS}	±10	V
Source Current (DC)	I_S	6	A
Source Current (Pulse) Note1	I_{SM}	60	A
Maximum Power Dissipation	P_D	1.1	W
Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃

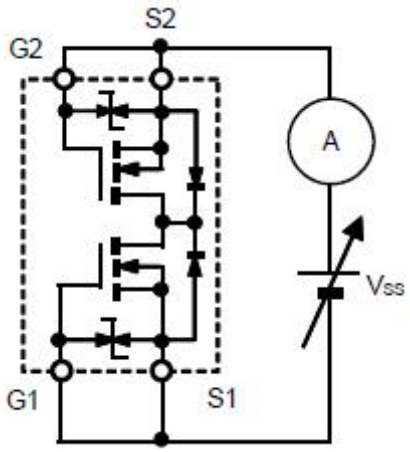
Note1:PW≤10μs, duty cycle≤1%;

ELECTRICAL CHARACTERISTICS (TA=25℃unless otherwise noted)

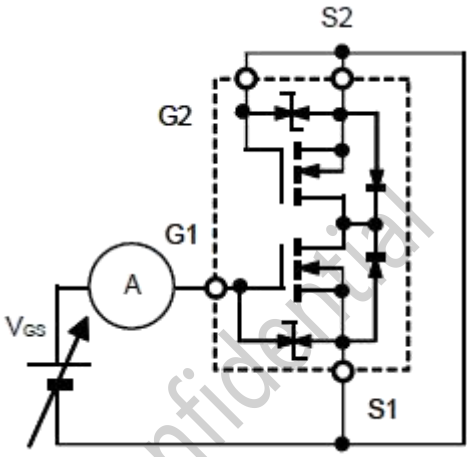
Parameter	Symbol	Condition	Min	Typ	Ma	Unit
Off Characteristics						
Source -Source Breakdown	BV_{SSS}	V_{GS}=0V ,I_S=250μA	12	-	-	V
Zero Gate Voltage Source Current	I_{SSS}	VSS=20V,VGS=0V TEST CIRCUIT 1	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±10V,V_{SS}=0V TEST CIRCUIT 2	-	-	±10	μA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	V_{SS}=V_{GS},I_S=250mA TEST CIRCUIT 3	0.5	0.8	1.2	V
Source -Source On-State Resistance	$R_{SS(ON)}$	V_{GS}=4.5V, I_S=3A	10	13.5	17	mΩ
		V_{GS}=4.0V, I_S=3A	11	14.2	18	mΩ
		V_{GS}=3.1V, I_S=3A	12	16	20	mΩ
		V_{GS}=2.5V, I_S=3A	14	20	25	mΩ
		TEST CIRCUIT 5				
Forward Transconductance	g_{FS}	V_{SS}=10V,I_S=1.8A TEST CIRCUIT 4	-	9	-	S
Dynamic Characteristics						
Input Capacitance	C_{lss}	V_{SS}=10V,V_{GS}=0V, F=1.0MHz TEST CIRCUIT 7	-	1313	-	pF
Output Capacitance	C_{oss}		-	257	-	pF
Reverse Transfer Capacitance	C_{rss}		-	238	-	pF
Switching Characteristics						
Turn-on Delay Time	$t_{d(on)}$	V_{SS}=10V,I_S=3A V_{GS}=4.5V, R_{GEN}=6Ω , R_L=3.3Ω TEST CIRCUIT 8	-	680	-	nS
Turn-on Rise Time	t_r		-	2960	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	6480	-	nS
Turn-Off Fall Time	t_f		-	6760	-	nS
Total Gate Charge	Qg(TOT)	V_{SS}=10V, I_S=6A, V_{GS}=4.5V TEST CIRCUIT 9	-	17.8	-	nC
Threshold Gate Charge	Qg(TH)		-	0.79	-	nC
Gate-Source Charge	Q_{gs}		-	2.5	-	nC
Gate-Drain Charge	Q_{gd}		-	6.4	-	nC
Body Diode Characteristics						
Body Diode Forward Voltage	V_{FSS}	V_{GS}=0V,I_F=1.0A TEST CIRCUIT 6	-	0.9	1.5	V

Both the FET1 and the FET2 are measured. Test circuits are example of measuring the FET1 side.

TEST CIRCUIT 1: ISS

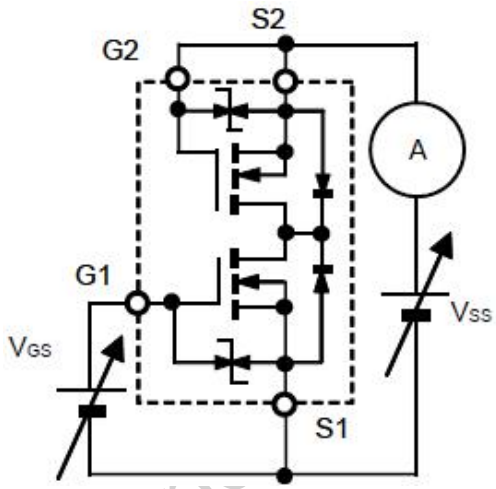


TEST CIRCUIT 2: IGSS



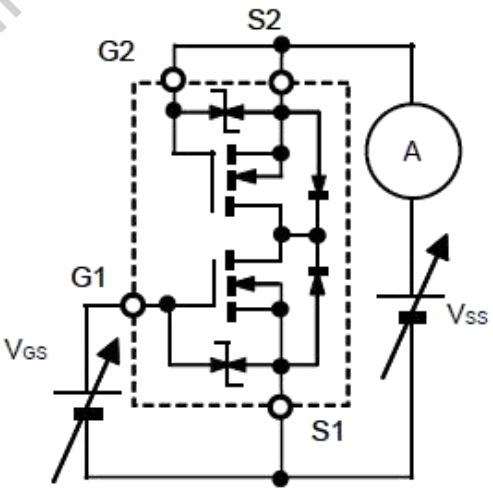
When FET1 is measured, between GATE and SOURCE of FET2 are shorted.

TEST CIRCUIT 3: VGS(off)



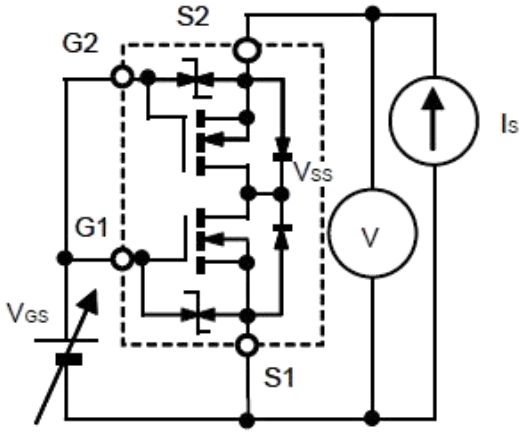
When FET1 is measured, between GATE and SOURCE of FET2 are shorted.

TEST CIRCUIT 4: GFS



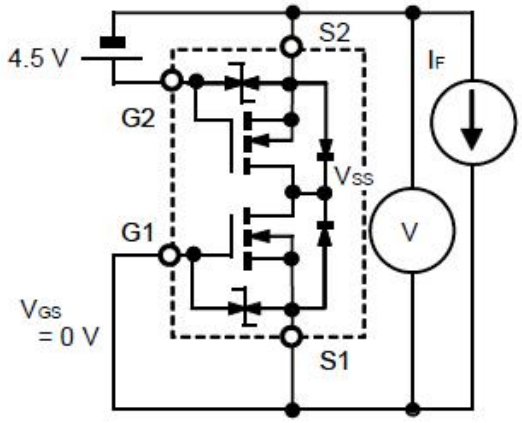
ΔIS/ΔVGS

TEST CIRCUIT 5 RSS(on)



VSS/IS

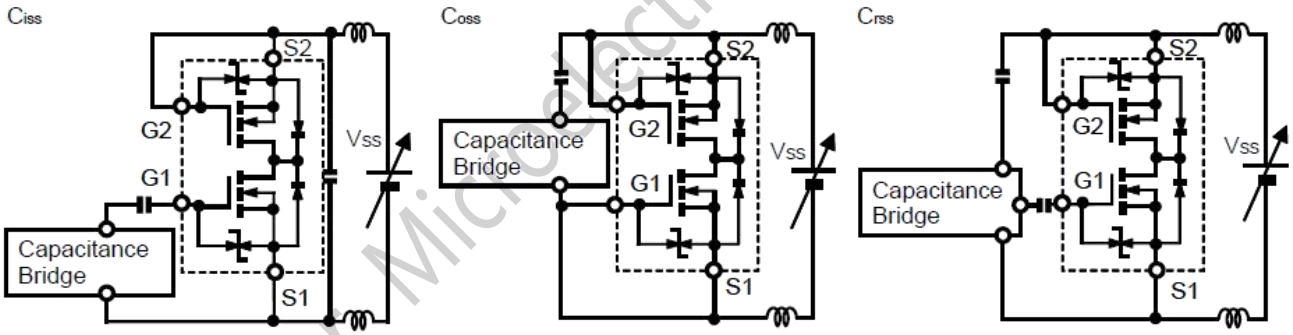
TEST CIRCUIT 6 VF(S-S)



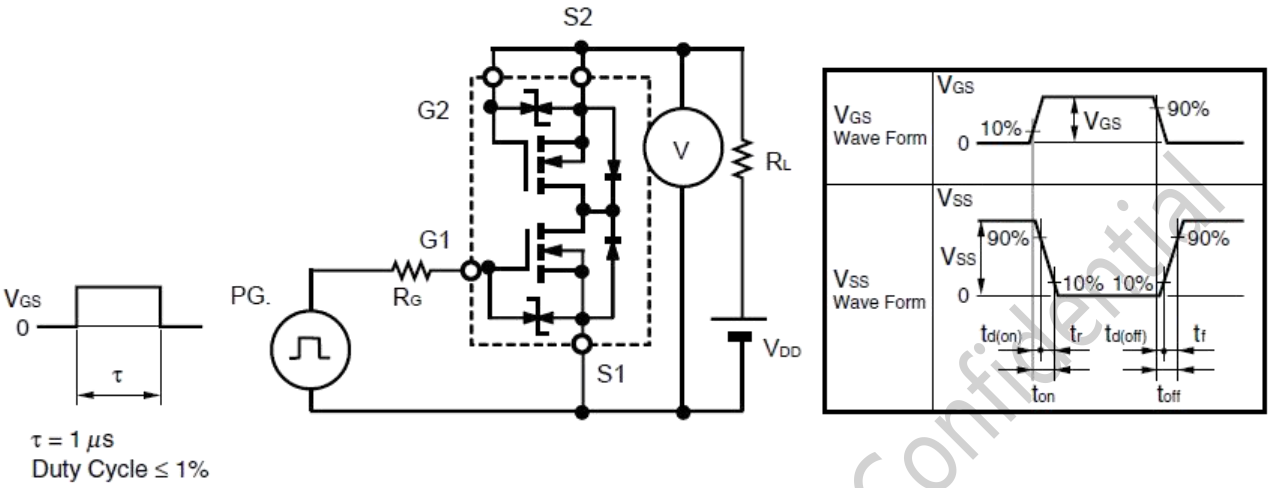
When FET1 is measured, FET2 is added VGS

+4.5 V.

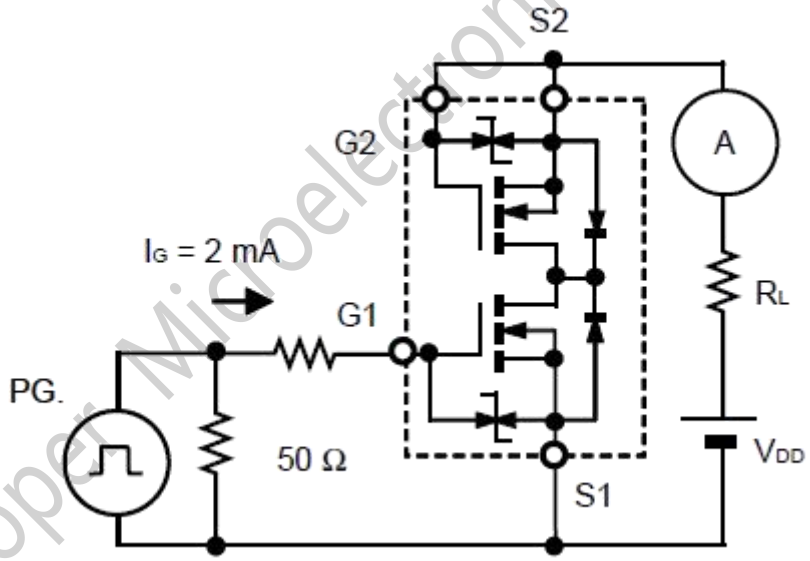
TEST CIRCUIT 7



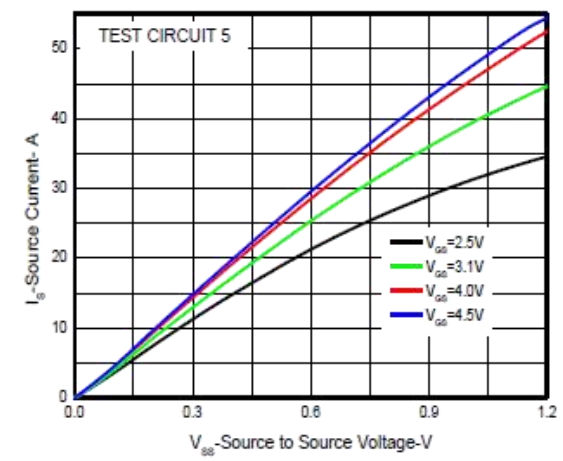
TEST CIRCUIT 8 td(on), tr, td(off), tf



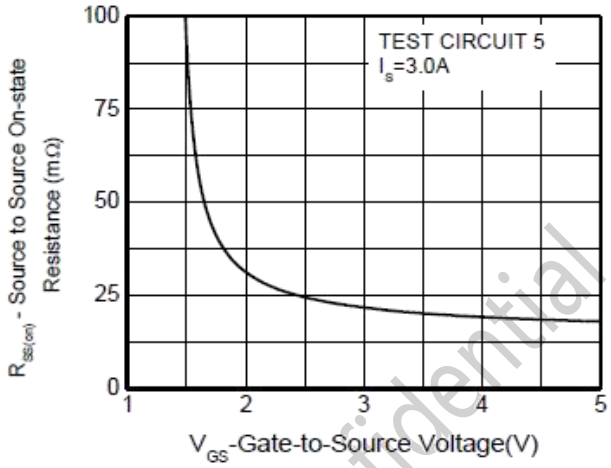
TEST CIRCUIT 9 QG



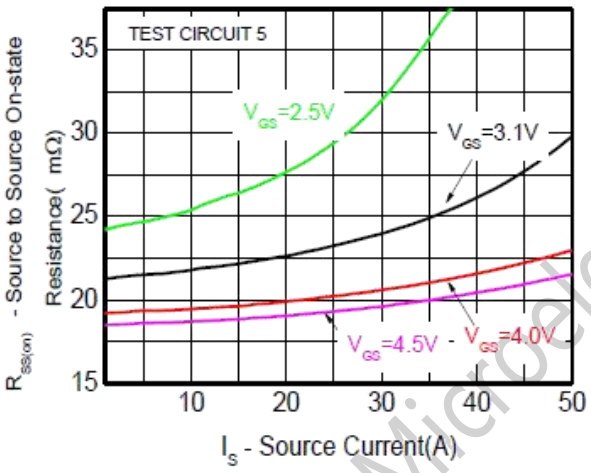
TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



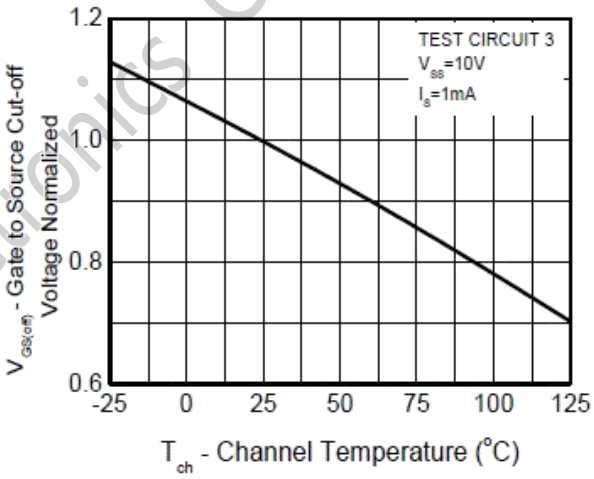
SOURCE CURRENT vs.
SOURCE TO SOURCE VOLTAGE



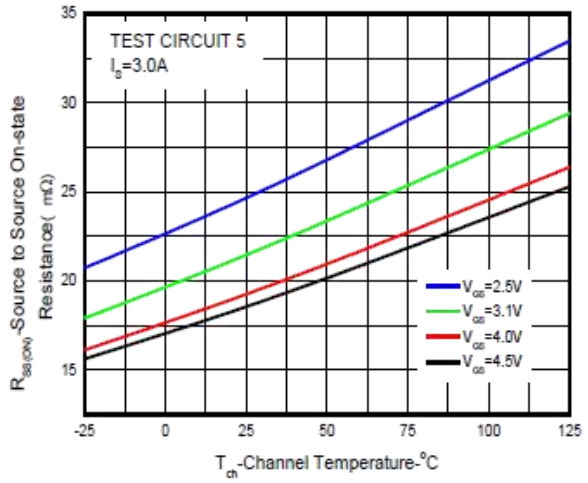
SOURCE TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



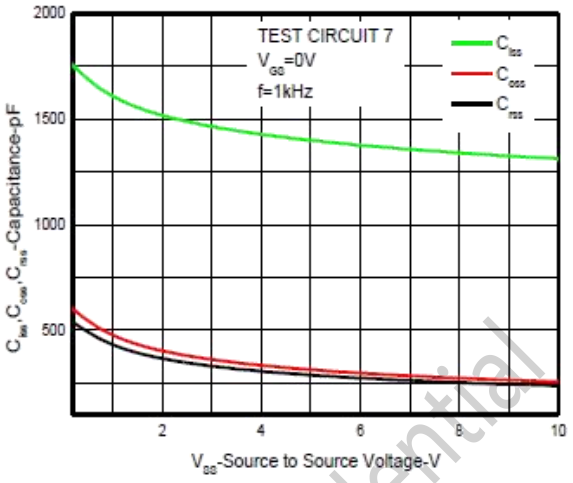
SOURCE TO SOURCE ON-STATE RESISTANCE vs.
SOURCE CURRENT



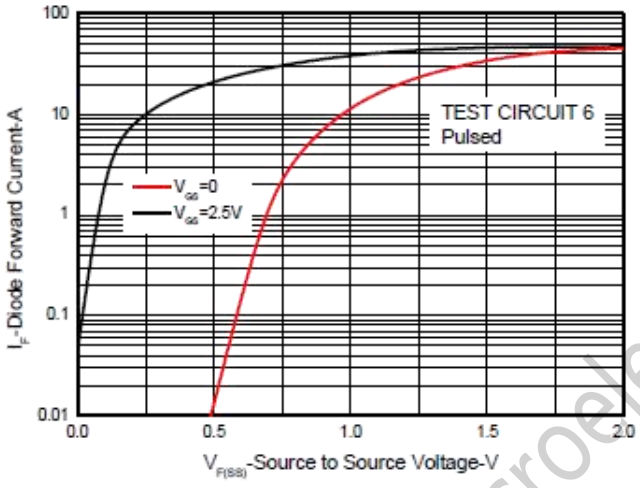
GATE TO SOURCE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



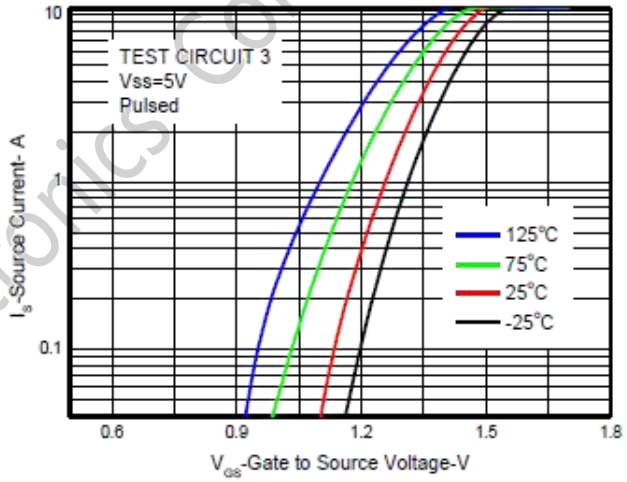
SOURCE TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



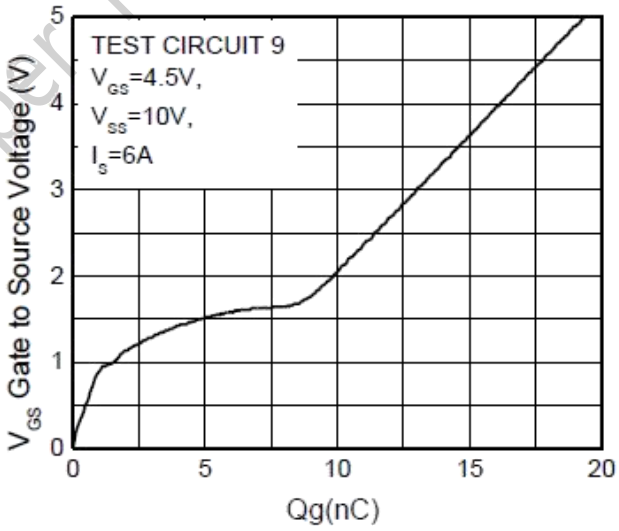
CAPACITANCE vs. SOURCE TO SOURCE VOLTAGE



SOURCE TO SOURCE DIODE FORWARD VOLTAGE



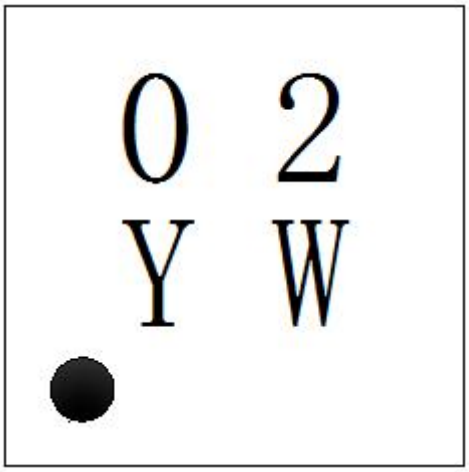
FORWARD TRANSFER CHARACTERISTICS



DYNAMIC INPUT CHARACTERISTICS

MARKING DESCRIPSION

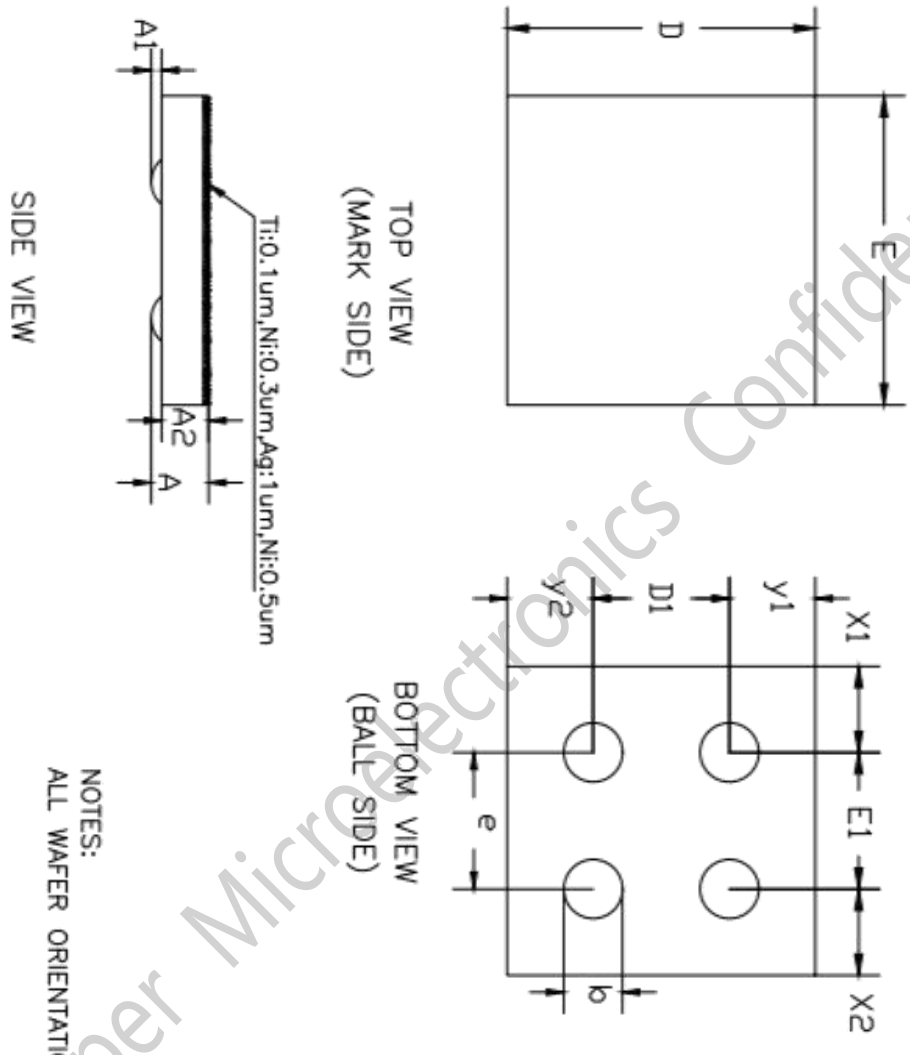
CSP-4L



NOTE:
02 —Part number of Product
Y —Code of productive year code(the last number of the year)
W —Code of productive week(A-Z:1-26 week; a-z:27-52week)

FOR EXCAMPLE:
02
7c
Means this product was produced in the 29th week of 2017

PACKAGE OUTLINE DIMENSIONS



NOTES:
ALL WAFER ORIENTATION NOTCH DOWN

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.220	0.250	0.280
A1	0.040	0.050	0.060
A2	0.180	0.200	0.220
D	1.450	1.470	1.490
D1		0.650BSC	
E	1.450	1.470	1.490
E1		0.650BSC	
b	0.260	0.280	0.300
e		0.650BSC	
x1		0.410 REF	
x2		0.410 REF	
y1		0.410 REF	
y2		0.410 REF	

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