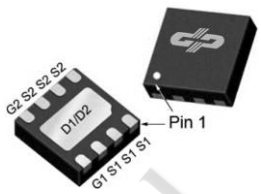
Product Summary

V_{DS}	20V	I_D	15A
$R_{DS(on).typ}$		4.6mΩ	V_{GS}=4.5V
		4.7mΩ	V_{GS}=3.9V
		5.6mΩ	V_{GS}=2.5V
		8.2mΩ	V_{GS}=1.8V

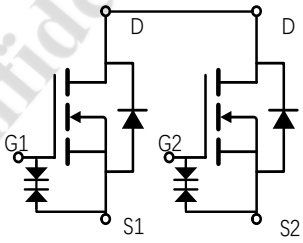
DFN3X3-8L



ESD rating, HBM 2000V

Features

DP8208 uses advanced trench technology to provide excellent RDS(ON), low gate charge and operation with gate voltages as low as 2.5V. It is ESD protected. This device is suitable for use as a Battery protection or in other Switching application.



Package Marking and Ordering Information

Part #	Marking	Package	Packing
DP8208	DP8208	DFN3X3	Reel

Halogen-Free

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	20	V
Continuous drain current T_C = 25°C (Silicon limit) T_C = 100°C (Silicon limit)	I_D	 15 10	A
Pulsed drain current (T_C = 25°C, t_p limited by T_{jmax})	$I_{D\ pulse}$	60	A
Gate-Source voltage	V_{GS}	±8	V
Power dissipation (T_C = 25°C)	P_{tot}	2	W
Lead Temperature for Soldering Purposes(1/8’’ from case for 10s	T_L	260	°C
Operating junction and storage temperature	T_j , T_{stg}	-55...+150	°C

[1].EAS is tested at starting Tj = 25°C, VGS = 5V.

Thermal Resistance

Parameter	Symbol	Max	Unit
Thermal resistance, junction – ambient(min. footprint)	R_{thJA}	61	°C/W

Electrical Characteristic (at Tj = 25 °C, unless otherwise specified)

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Static Characteristic						
Drain-source breakdown voltage	BV_{DSS}	20	-	-	V	V_{GS}=0V, I_D=250uA
Gate threshold voltage	$V_{GS(th)}$	0.4	0.7	1	V	V_{DS}=V_{GS},I_D=250uA
Zero gate voltage drain current	I_{DSS}	- -	- -	1 100	μA	V_{DS}=16V,V_{GS}=0V T_j=25°C T_j=125°C
Gate-source leakage current	I_{GSS}	-	-	±10	μA	V_{GS}=±8V,V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	 4.6 4.7 5.6 -	 6.0 6.2 6.5 12.0		mΩ	T_j=25°C V_{GS}=4.5V, I_D=3A V_{GS}=3.9V, I_D=3A V_{GS}=2.5V, I_D=3A V_{GS}=1.8V, I_D=3A
Transconductance[2]	g_{fs}	-	45	-	S	V_{DS}=5V,I_D=3A
Dynamic Characteristic[2]						
Input Capacitance	C_{iss}	-	4350	-	pF	V_{GS}=0V, V_{DS}=10V, f=1MHz
Output Capacitance	C_{oss}	-	396	-		
Reverse Transfer Capacitance	C_{rss}	-	255	-		
Gate Total Charge	Q_g	-	59	-	nC	V_{GS}=4.5V, V_{DS}=10V, I_D=3A, f=1MHz
Gate-Source charge	Q_{gs}	-	18	-		
Gate-Drain charge	Q_{gd}	-	12	-		
Turn-on delay time	$t_{d(on)}$	-	1.2	-	μs	V_{GS}=4.5V, V_{DD}=10V, R_{G_ext}=2.7Ω
Rise time	t_r	-	2.4	-		
Turn-off delay time	$t_{d(off)}$	-	8.1	-		
Fall time	t_f	-	3.9	-		

Body Diode Characteristic

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Body Diode Forward Voltage	V_{SD}	-	0.8	1.2	V	V_{GS}=0V,I_{SD}=3A
Diode continuous forward current	I_s	-	15	-	A	TC = 25°C
Diode pluse current	$I_{s\ pluse}$	-	60	-	A	TC = 25°C

[2]. Defined by design. Not subject to production test

Typical Performance Characteristics

Fig 1: Output Characteristics

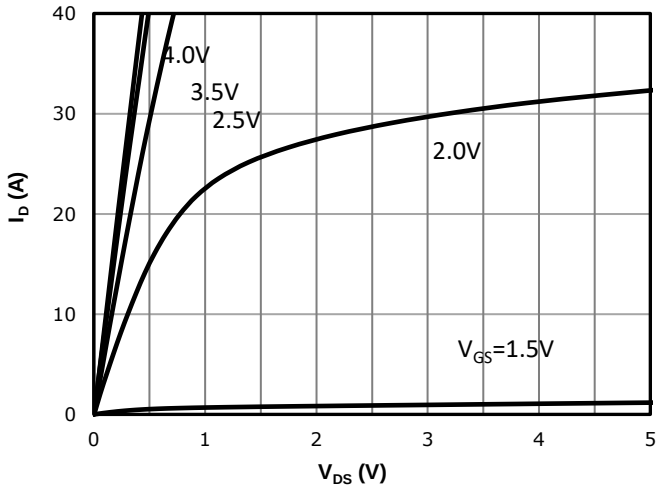


Fig 2: Transfer Characteristics

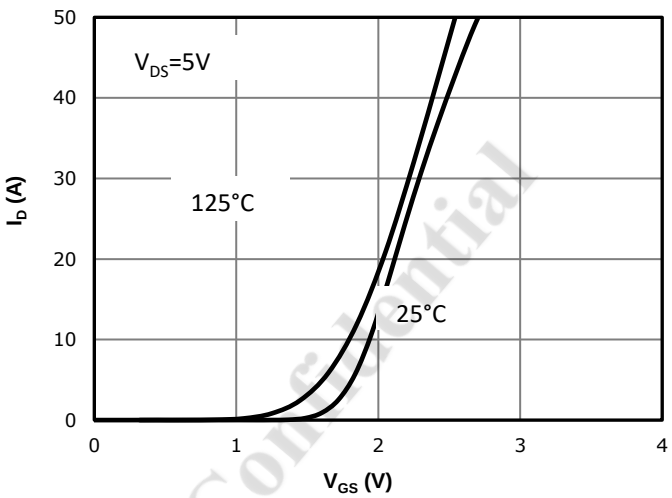


Fig 3: Rds(on) vs Drain Current and Gate Voltage

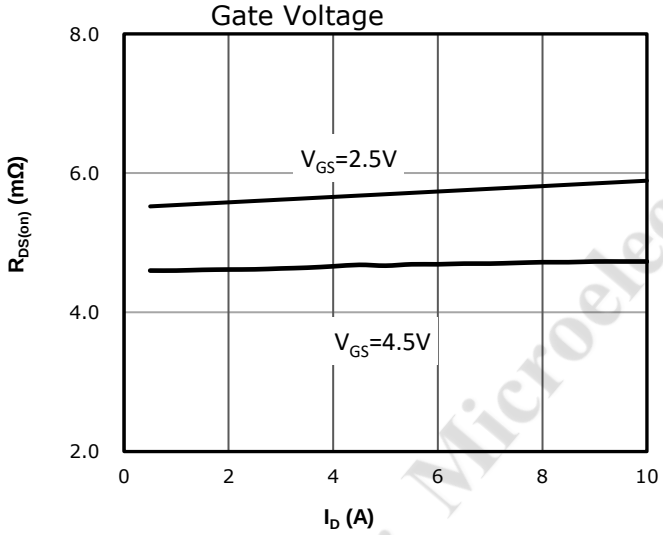


Fig 4: Rds(on) vs Gate Voltage

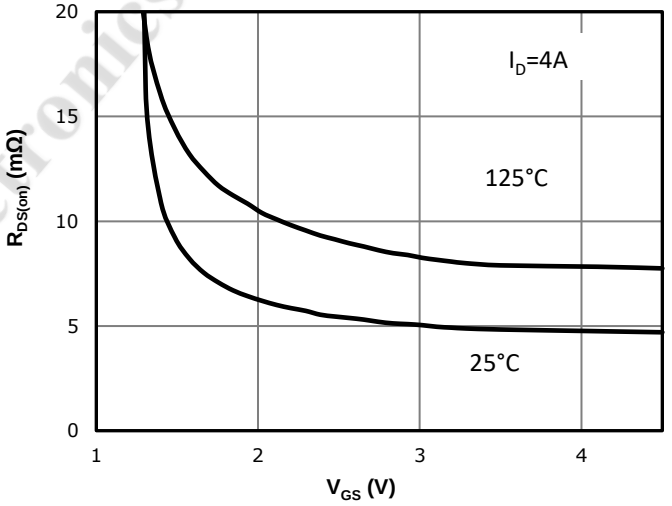


Fig 5: Rds(on) vs. Temperature

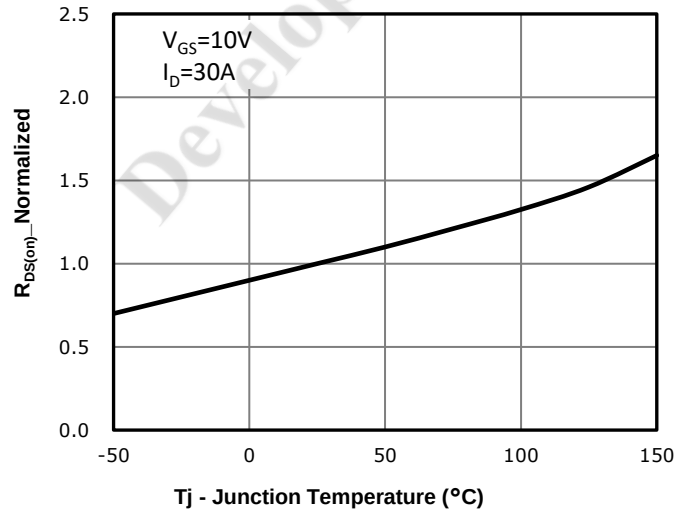


Fig 6: Capacitance Characteristics

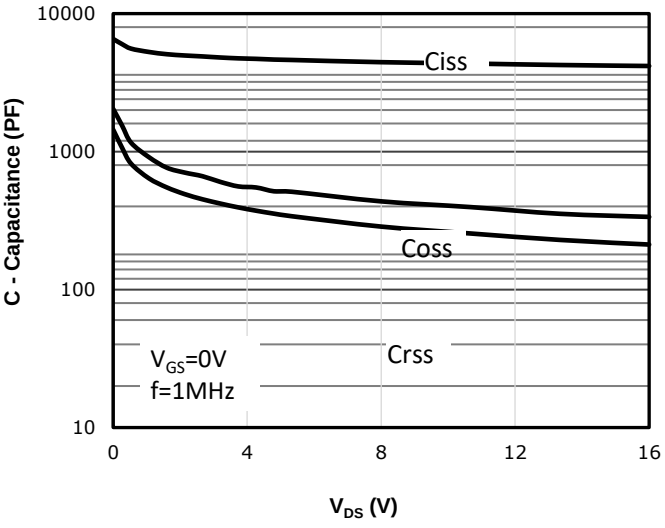


Fig 7: Gate Charge Characteristics

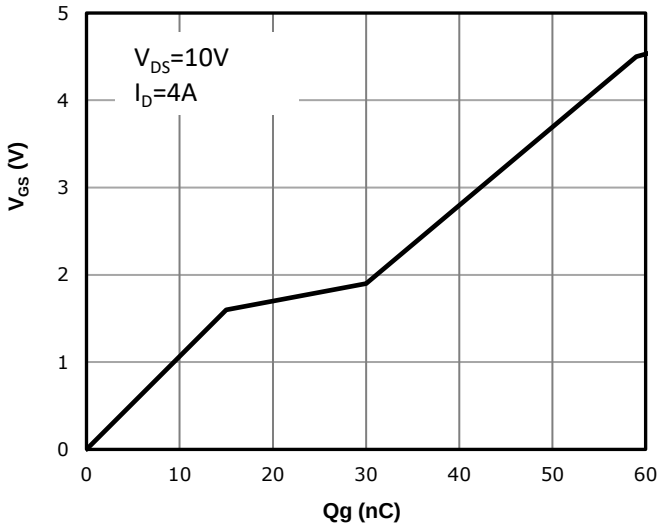


Fig 8: Body-diode Forward Characteristics

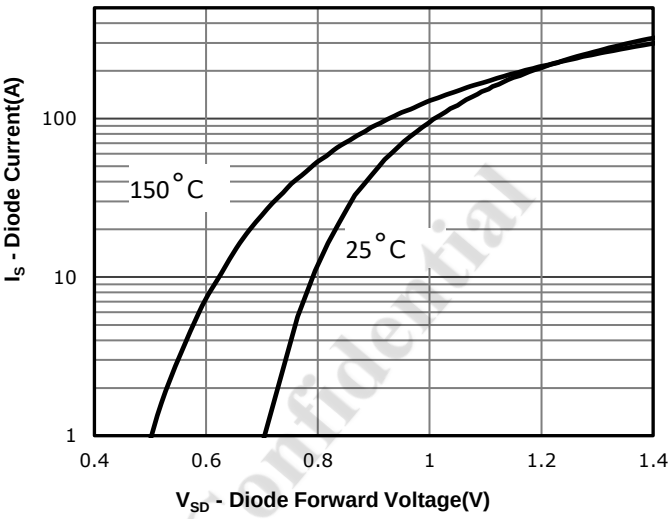


Fig 9: Safe Operating Area

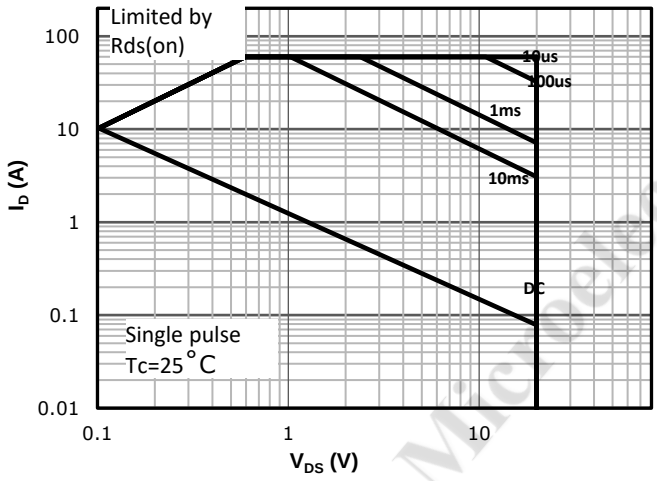
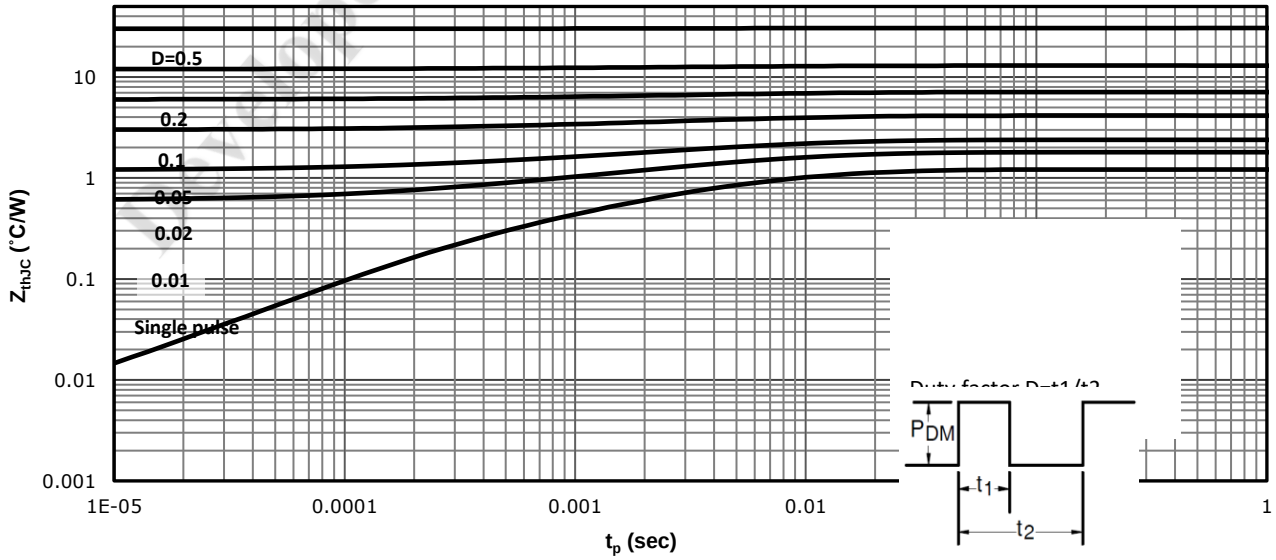
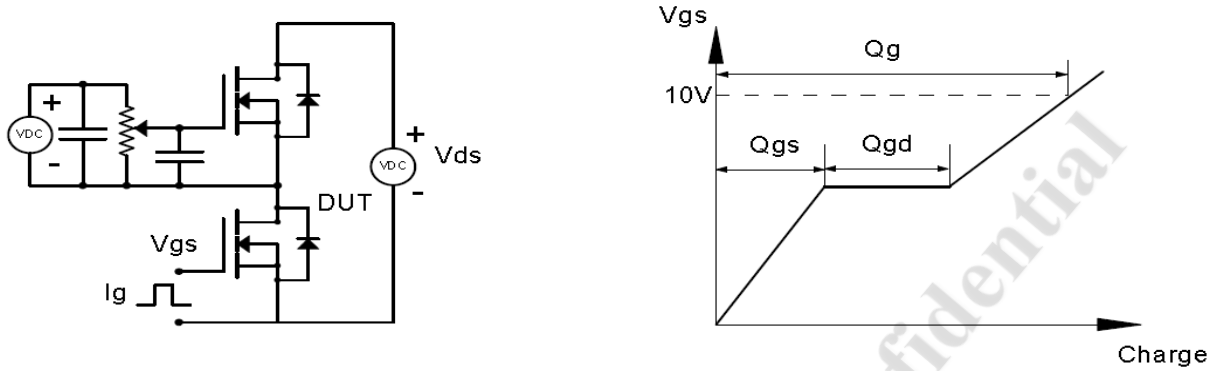


Fig 10: Max. Transient Thermal Impedance

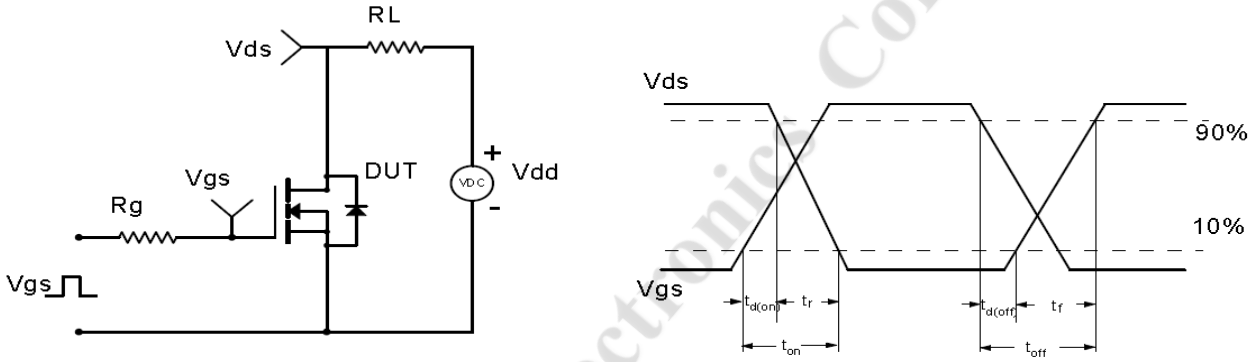


Test Circuit & Waveform

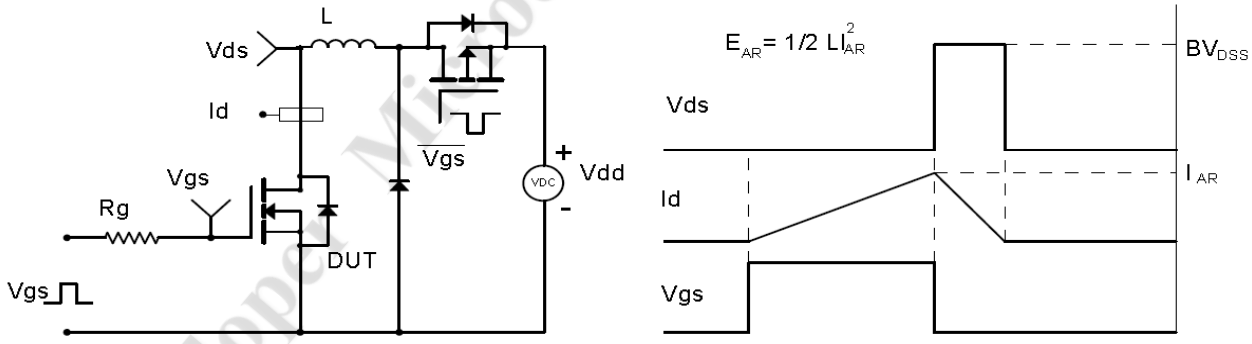
Gate Charge Test Circuit & Waveform



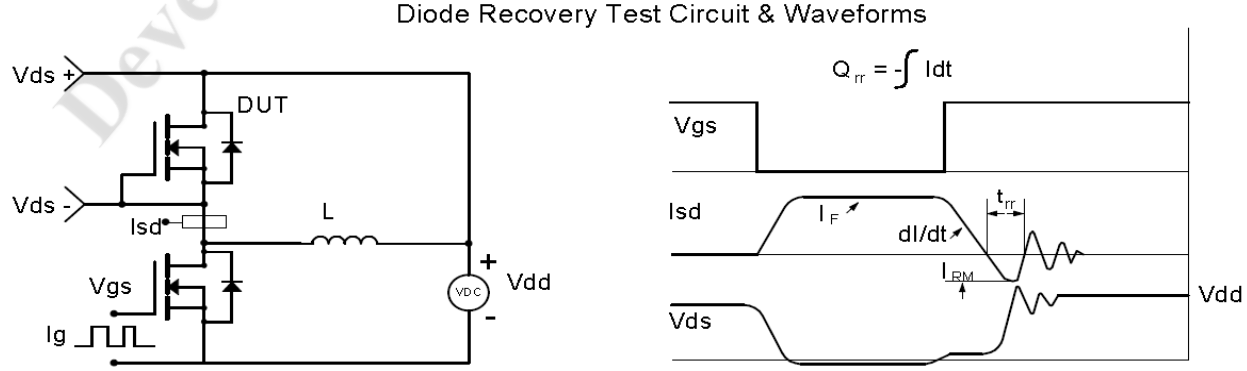
Resistive Switching Test Circuit & Waveforms



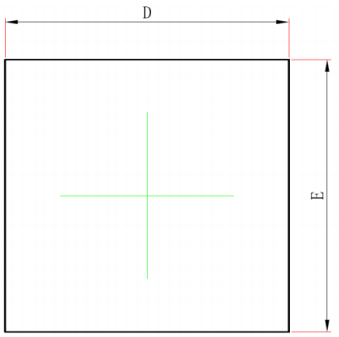
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



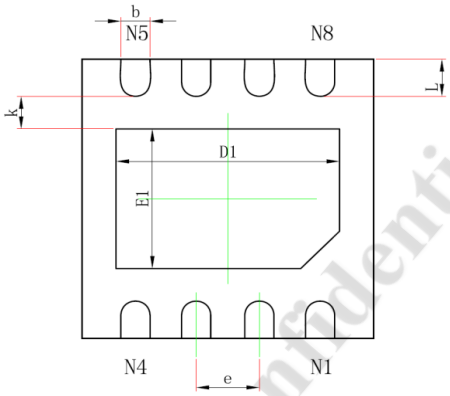
Diode Recovery Test Circuit & Waveforms



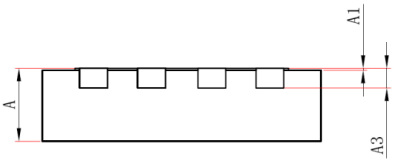
Package Outline: DFN3X3-8L



TOP VIEW



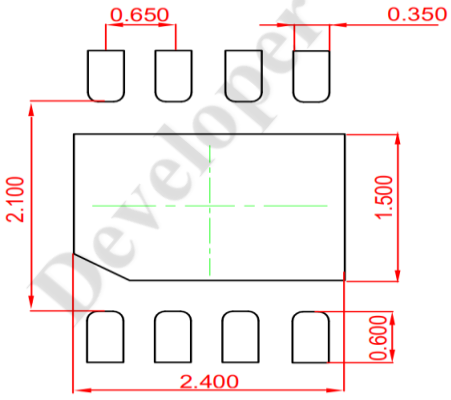
BOTTOM VIEW



SIDE VIEW

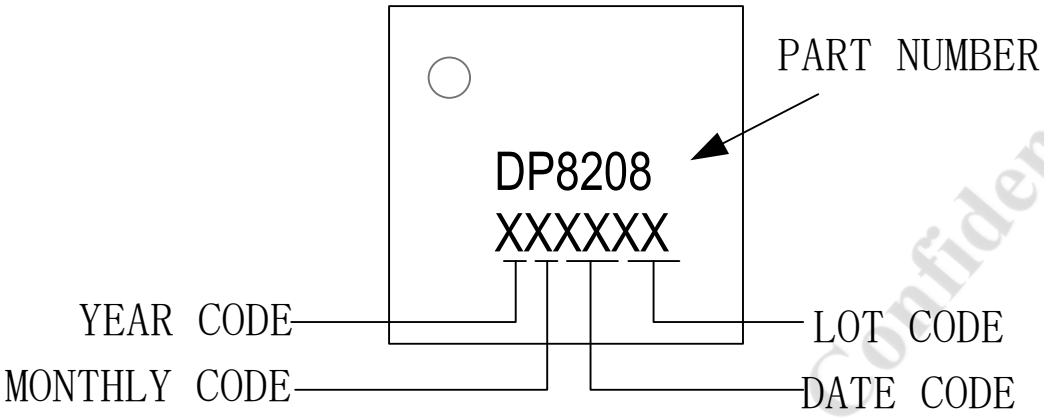
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	2.924	3.076	0.115	0.121
E	2.924	3.076	0.115	0.121
D1	2.200	2.400	0.087	0.094
E1	1.400	1.600	0.055	0.063
b	0.250	0.350	0.010	0.014
k	0.200MIN		0.008MIN	
e	0.650TYP.		0.026TYP.	
L	0.324	0.476	0.013	0.019

Recommended land pattern



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.050mm.
3.The pad layout is for reference purposes only.

Part Marking Information



Revision History

Revison	Major changes
1.6	Release for formal version1.6

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