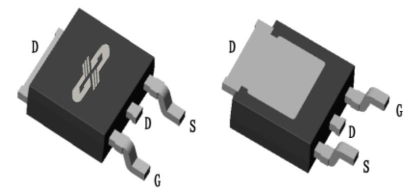
DP070N02DTL

TRMOS N-MOSFET 20V, 4.8mΩ, 60A

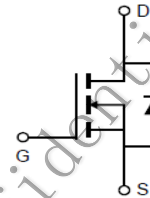
Product Summary

Part #	V_{DS}	$R_{DS(on).typ}$ (@V_{GS}=4.5V)	$R_{DS(on).typ}$ (@V_{GS}=2.5V)	I_D
DP070N02DTL	20V	4.8mΩ	6.7mΩ	60A



Features

- Advanced high cell density Trench MOSFET technology
- Better $R_{DS(on)}$ enabled by a low $R_{DSon.sp}$, low conduction losses
- Excellent Q_gx$R_{DS(on)}$ product(FOM)
- Qualified according to JEDEC criteria



100% Avalanche Tested

100% Rg Tested

Applications

- Battery management
- Power Management Switches

Package Marking and Ordering Information

Part #	Marking	Package	Packing
DP070N02DTL	070N02DT	TO-252	Tube/Reel

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	20	V
Continuous drain current T_C = 25°C (Silicon limit) T_C = 25°C (Package limit) T_C = 100°C (Silicon limit)	I_D	71 60 45	A
Pulsed drain current (T_C = 25°C, t_p limited by T_{jmax})	$I_{D\ pulse}$	240	A
Avalanche energy, single pulse (I=0.3mH, Rg=25)[1]	E_{AS}	97	mJ
Gate-Source voltage	V_{GS}	±10	V
Power dissipation (T_C = 25°C)	P_{tot}	52	W
Operating junction and storage temperature	T_j , T_{stg}	-55...+150	°C

[1].EAS is tested at starting T_j = 25°C, V_{GS} = 10V.

Thermal Resistance

Parameter	Symbol	Max	Unit
Thermal resistance, junction – case.	R_{thJC}	2.40	°C/W
Thermal resistance, junction – ambient(min. footprint)	R_{thJA}	56	°C/W

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Electrical Characteristic (at Tj = 25 °C, unless otherwise specified)

Parameter	Symbol	Value min.	Value typ.	Value max.	Unit	Test Condition
Static Characteristic						
Drain-source breakdown voltage	BV_{DSS}	20	-	-	V	V_{GS}=0V, I_D=250uA
Gate threshold voltage	$V_{GS(th)}$	0.45	-	1	V	V_{DS}=V_{GS},I_D=250uA
Zero gate voltage drain current	I_{DSS}	- -	- -	1 100	μA	V_{DS}=16V,V_{GS}=0V T_j=25°C T_j=150°C
Gate-source leakage current	I_{GSS}	-	-	±100	nA	V_{GS}=±10V,V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	- -	4.8 6.7	6.0 9.0	mΩ mΩ	V_{GS}=4.5V, I_D=30A V_{GS}=2.5V, I_D=25A
Dynamic Characteristic[2]						
Input Capacitance	C_{iss}	-	1810	-	pF	V_{GS}=0V, V_{DS}=10V, f=1MHz
Output Capacitance	C_{oss}	-	280	-		
Reverse Transfer Capacitance	C_{rss}	-	256	-		
Gate Total Charge(V_{GS}=10V)	Q_g	-	23	-	nC	V_{GS}=10V, V_{DS}=10V, I_D=30A, f=1MHz
Gate Total Charge(V_{GS}=4.5V)	Q_g	-	14	-		
Gate-Source charge	Q_{gs}	-	4.5	-		
Gate-Drain charge	Q_{gd}	-	7.5	-		
Turn-on delay time	$t_{d(on)}$	-	15	-	ns	V_{GS}=4.5V, V_{DD}=10V, R_{G_ext}=2.7Ω
Rise time	t_r	-	30	-		
Turn-off delay time	$t_{d(off)}$	-	52	-		
Fall time	t_f	-	16.8	-		

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Body Diode Characteristic

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Body Diode Forward Voltage	V_{SD}	-	0.81	1.1	V	V_{GS}=0V,I_{SD}=30A
Diode continuous forward current	I_s	-	60	-	A	TC = 25°C
Diode pluse current	$I_{s\ pluse}$	-	240	-	A	TC = 25°C
Body Diode Reverse Recovery Time[2]	t_{rr}	-	21	-	ns	I_F=20A, dI/dt=100A/μs
Body Diode Reverse Recovery Charge[2]	Q_{rr}	-	26	-	nC	

[2]. Defined by design. Not subject to production test

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Typical Performance Characteristics

Fig 1: Output Characteristics

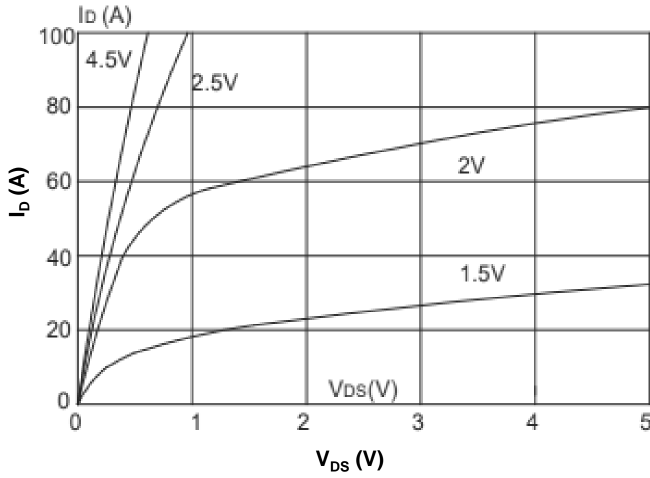

Fig 2: Transfer Characteristics

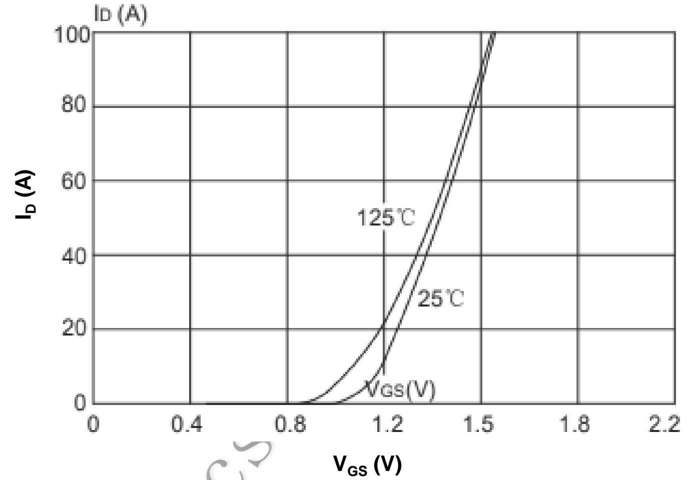

Fig 3: Rds(on) vs Drain Current and Gate Voltage

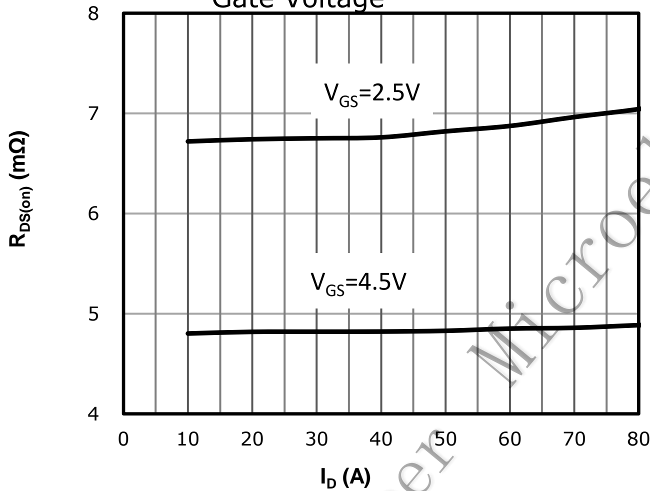

Fig 4: Rds(on) vs Gate Voltage

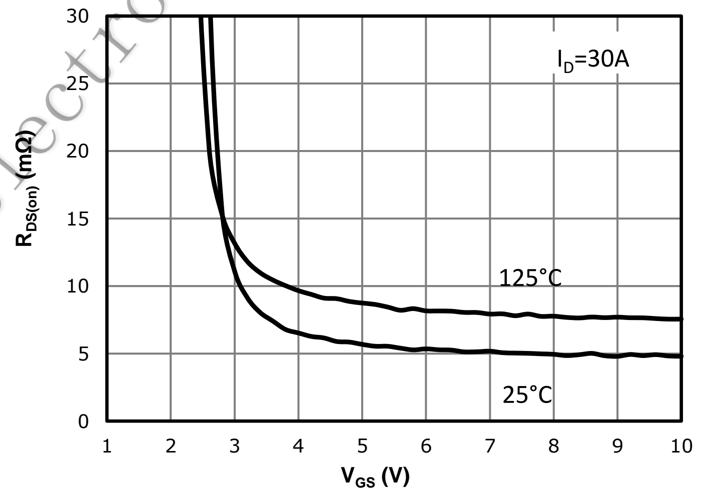

Fig 5: Rds(on) vs. Temperature

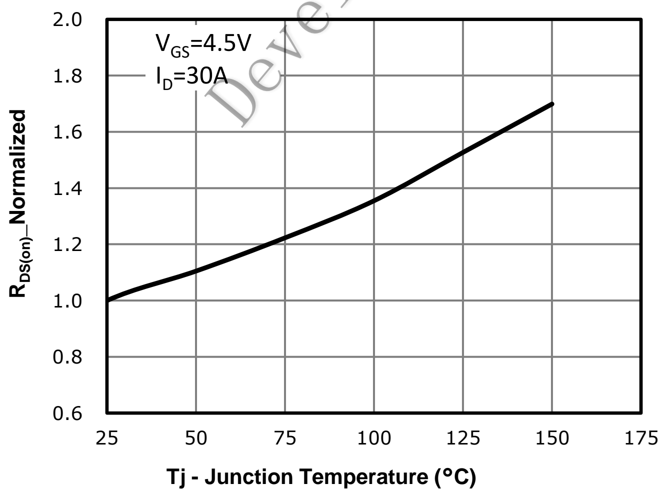

Fig 6: Capacitance Characteristics

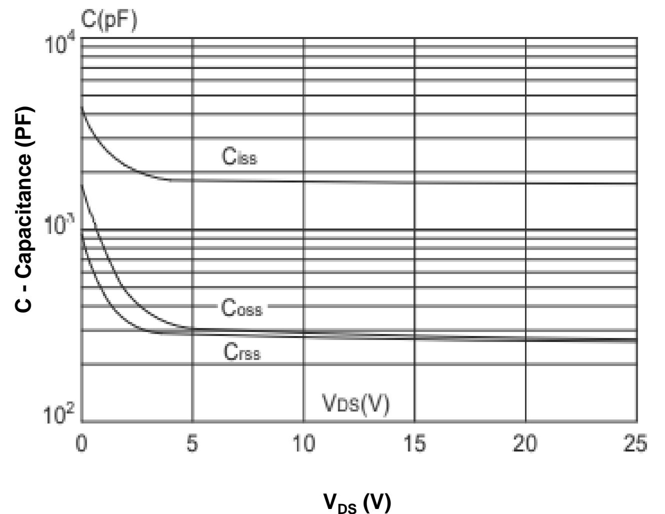

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Fig 7: Gate Charge Characteristics

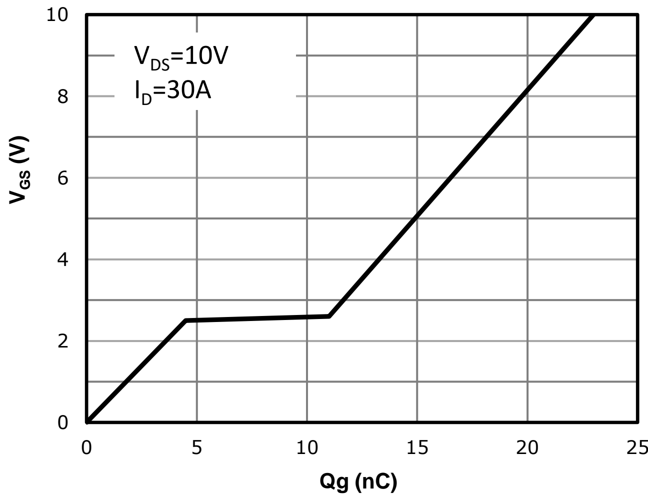

Fig 8: Body-diode Forward Characteristics

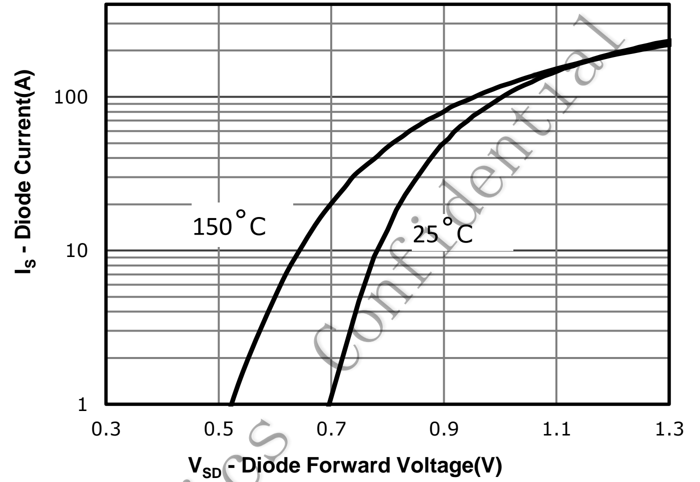

Fig 9: Power Dissipation

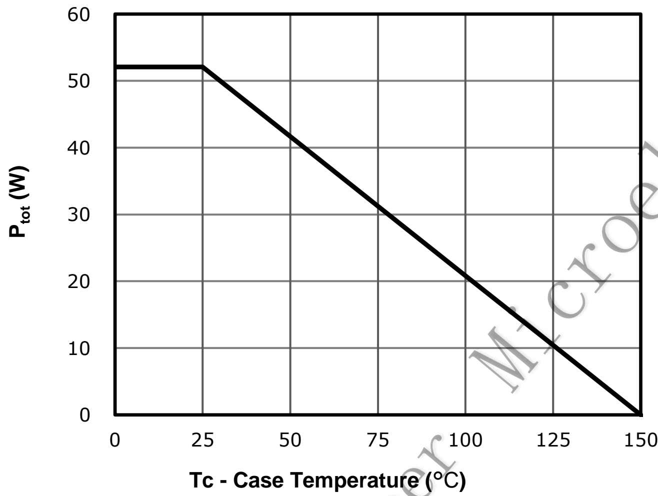

Fig 10: Drain Current Derating

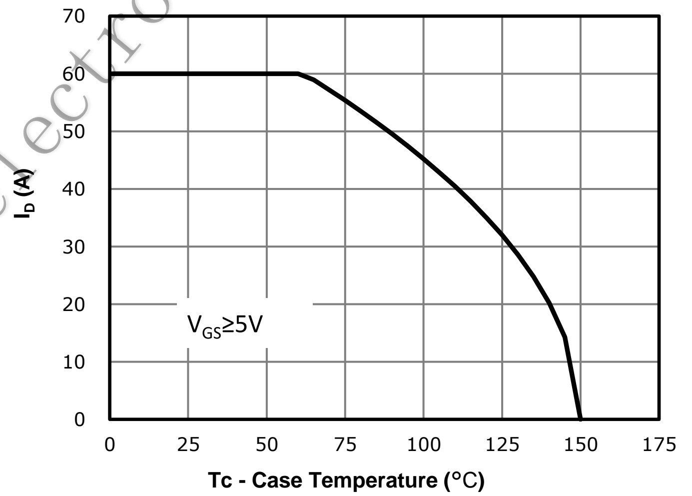

Fig 11: Safe Operating Area

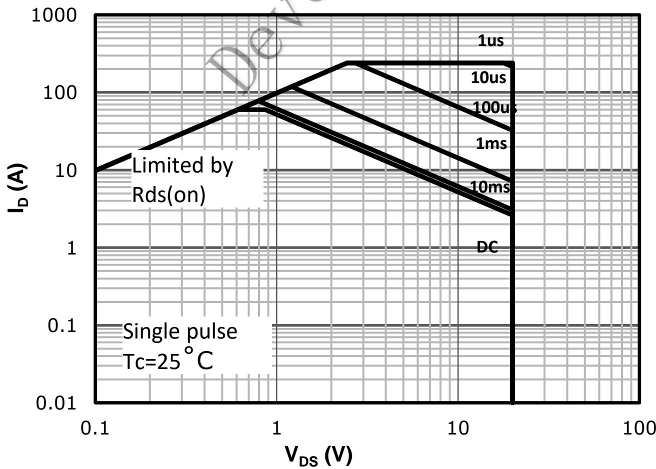

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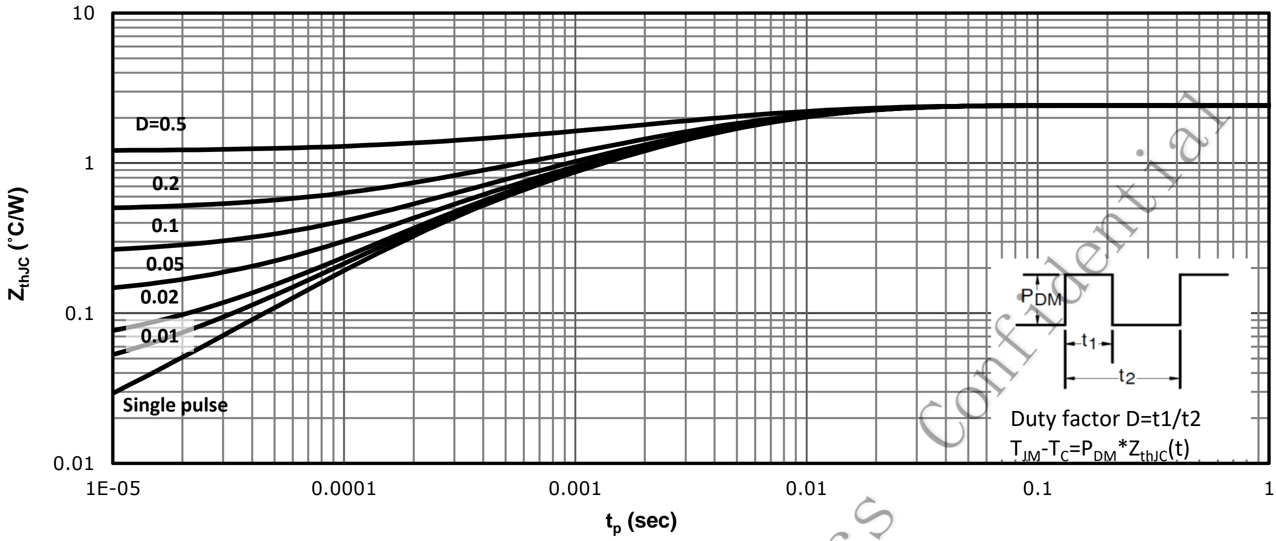
Fig 12: Max. Transient Thermal Impedance



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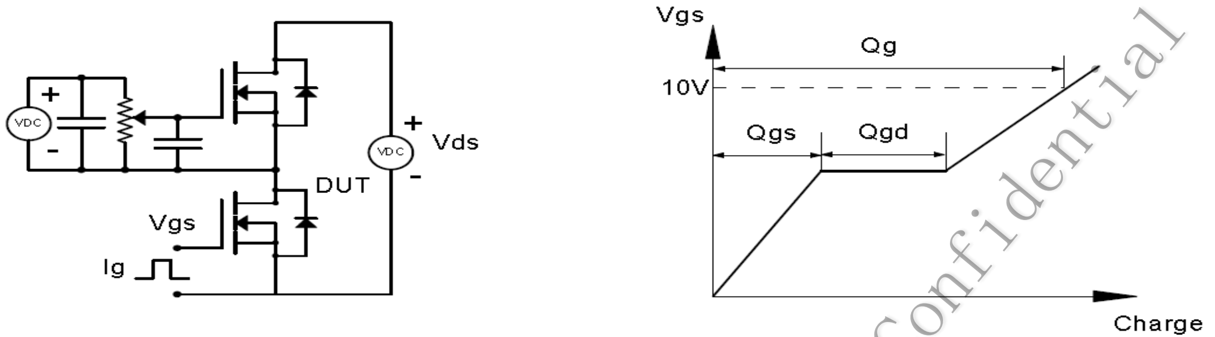
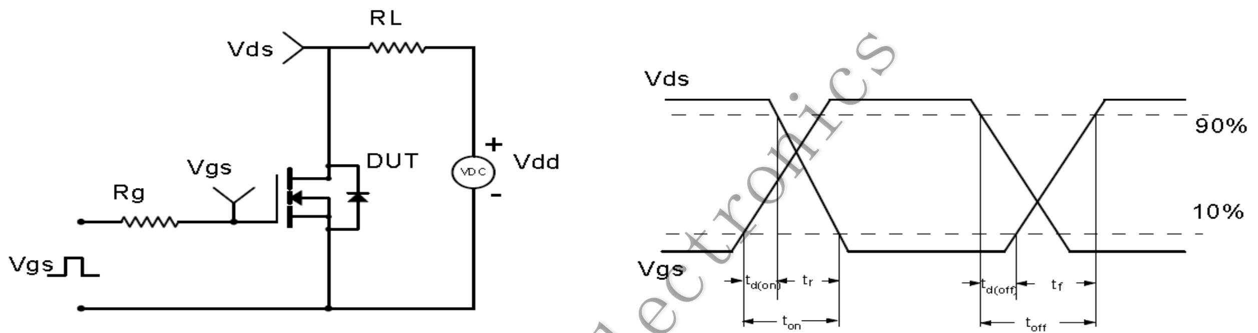
Test Circuit & Waveform

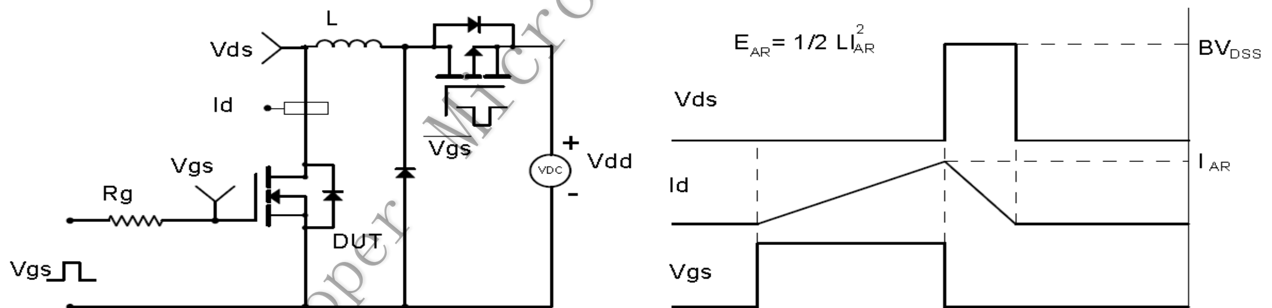
Gate Charge Test Circuit & Waveform



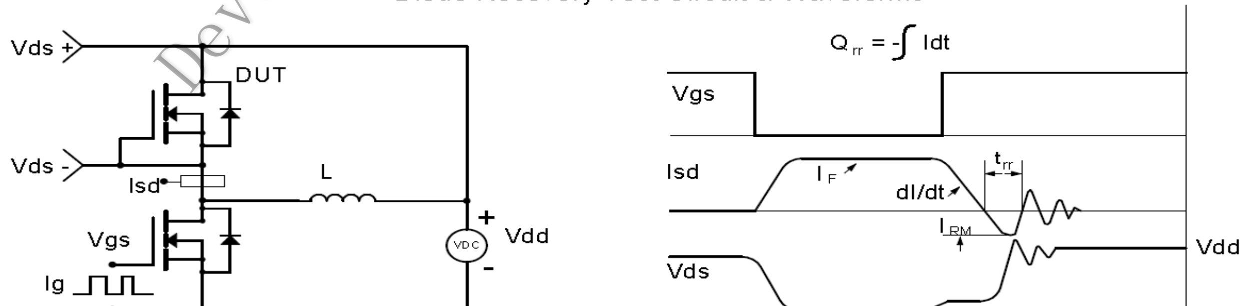
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



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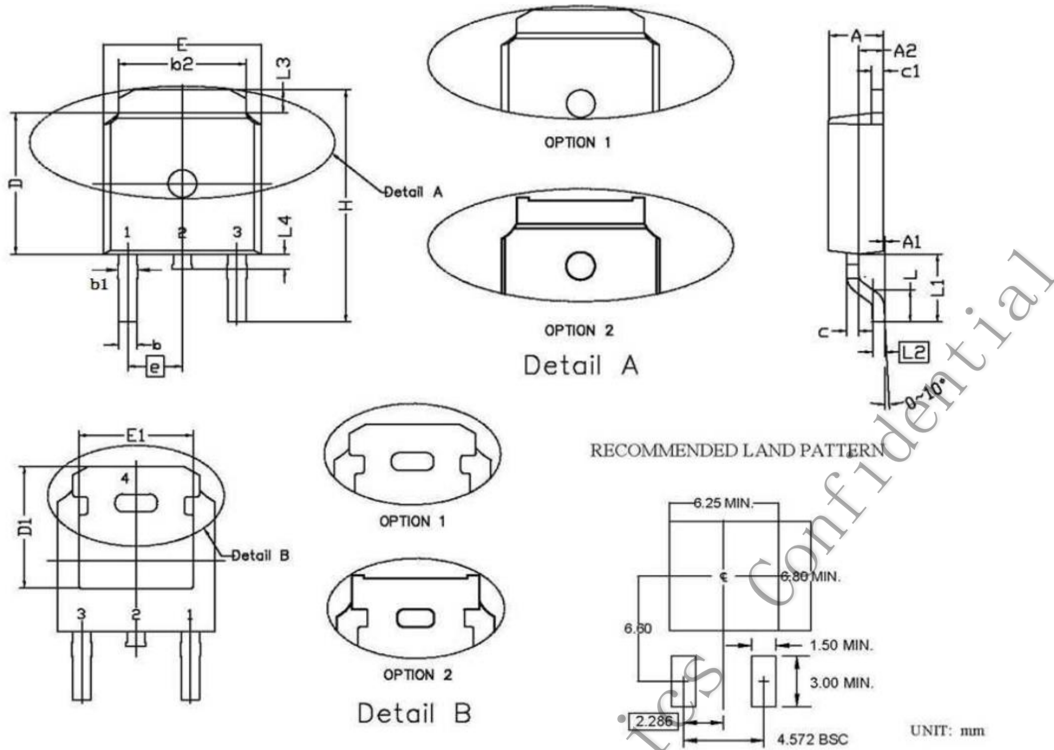
Package Outline: TO-252



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Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.15	2.45	0.085	0.096
A1	0.00	0.15	0.000	0.006
A2	0.76	1.36	0.030	0.054
b	0.60	0.91	0.024	0.036
b1	0.65	1.15	0.026	0.045
b2	5.00	5.64	0.197	0.222
c	0.45	0.61	0.018	0.024
c1	0.36	0.66	0.014	0.026
D	5.80	6.30	0.228	0.248
D1	5.00	6.00	0.197	0.236
e	2.29 BSC.		0.090 BSC.	
E	6.30	6.90	0.248	0.272
E1	4.55	5.30	0.179	0.209
H	9.40	10.48	0.370	0.413
L	1.18	1.70	0.046	0.067
L1	2.92 REF		0.115 REF	
L2	0.36	0.66	0.014	0.026
L3	0.72	1.35	0.028	0.053
L4	0.60	1.20	0.024	0.047

1.0	Release for formal version

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