Highly Integrated Offline Current Mode PWM Power Switch

FEATURES

- Integrated with 650V Power MOSFET
- ±1% CV Regulation
- Less than 75mW Standby Power
- Fixed 65KHz Switching Frequency
- Green Mode and Burst Mode Control
- Very Low Startup and Operation Current
- Built-in Frequency Shuffling to Reduce EMI
- Built-in Current Mode Control with Internal Slope Compensation
- Built-in Protections with Auto Recovery:
  - VDD Under Voltage Lockout (UVLO)
  - VDD Over Voltage Protection (OVP)
  - On-Chip Thermal Shutdown (OTP)
  - Cycle-by-Cycle Current Limiting
  - Over Load Protection (OLP)
  - CS Pin Float Protection
- Available with DIP8 Package

APPLICATIONS

- Power Adapter
- General Switch Mode Power Supply

GENERAL DESCRIPTION

DP2363 is a high performance current mode PWM power switch for offline flyback converter applications.

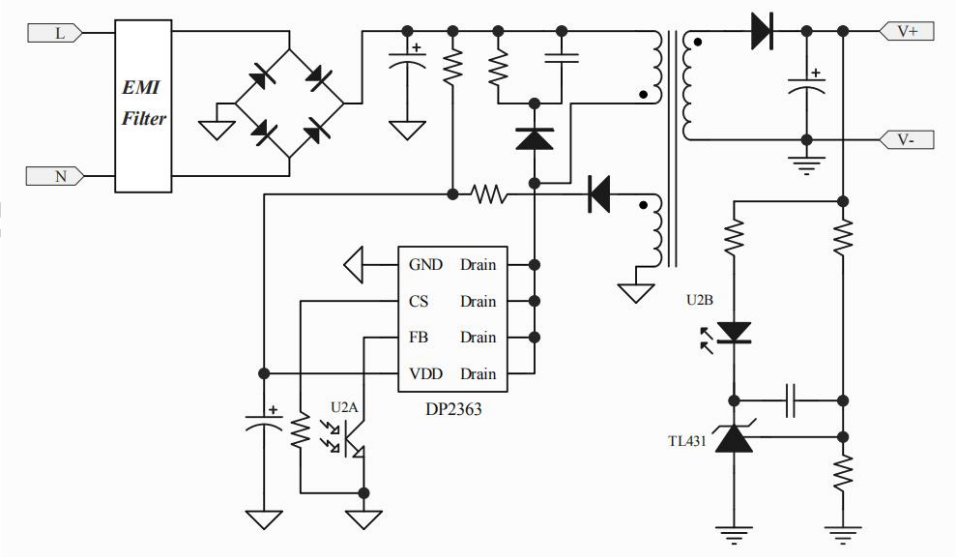
In DP2363, PWM switching frequency with shuffling is fixed to 65KHz and is trimmed to tight range. The IC has built-in green and burst mode control for light and zero loadings, which can achieve less than 75mW standby power.

DP2363 integrates functions and protections of Under Voltage Lockout (UVLO), VDD over Voltage Protection (VDD OVP), Cycle-by-cycle Current Limiting (OCP), Over Load Protection (OLP), On-Chip Thermal Shutdown (OTP), Soft Start, VDD Clamping and CS Pin Float Protection, etc.

ORDERING INFORMATION

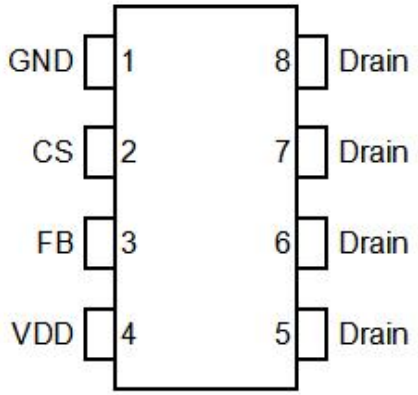
Part Number	Description
DP2363	DIP8,ROHS 50 Pcs/Tube

TYPICAL APPLICATION CIRCUIT



PRODUCT DESCRIPTION

➢ Pin Configuration



➢ Pin Description

Pin Number	Pin Number	I/O	Description
1	GND	P	The Ground of the IC
2	CS	I	Current Sense Input Pin
3	FB	I	Feedback pin. The loop regulation is achieved by connecting a photo-coupler to this pin. PWM duty cycle is determined by this pin voltage and the current sense signal at Pin 2
4	VDD	P	IC power supply pin
5,6.7.8	Drain	O	The Power MOSFET Drain

➢ Marking Information

DP2363 for product name;

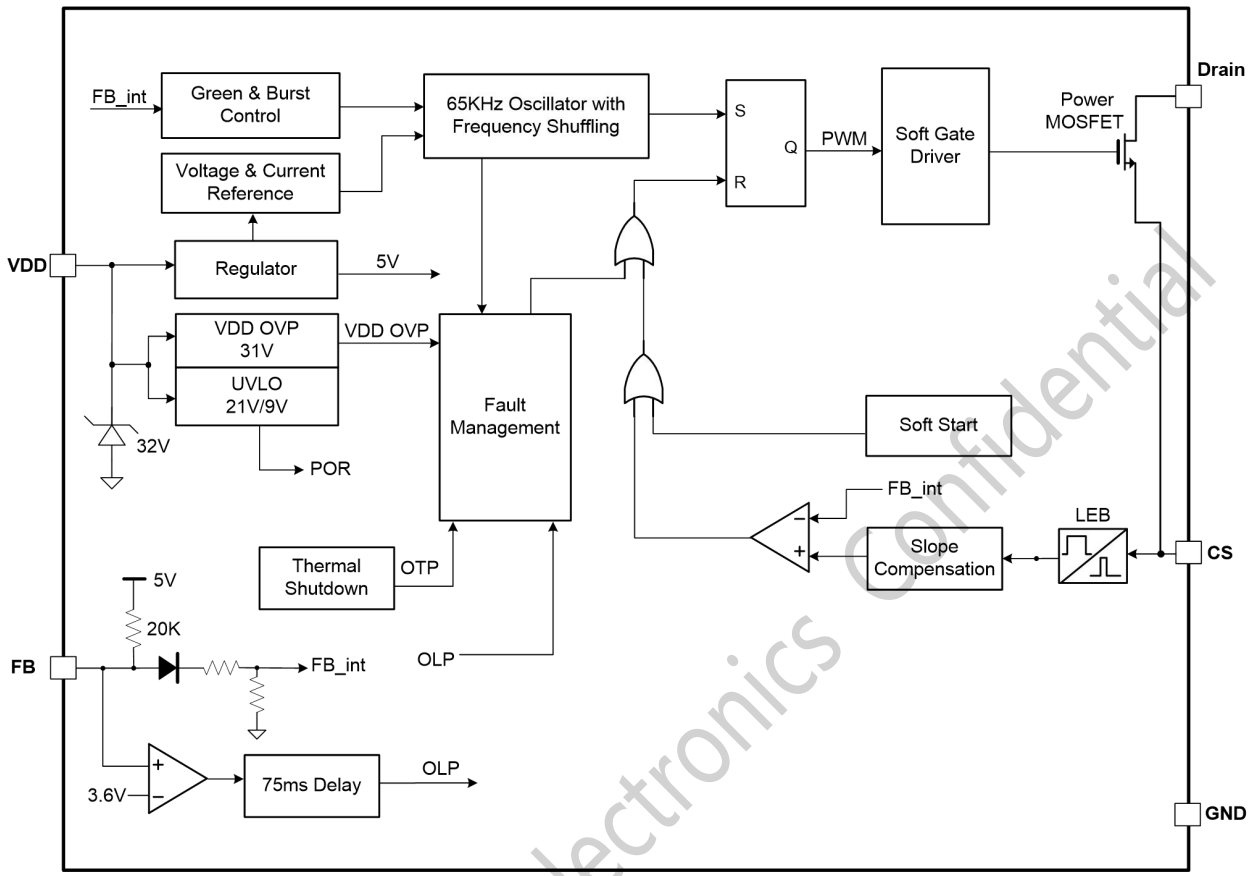
XXXXXX The first X represents the last year,2020 is 0; The second X represents the month, in A-L 12 letters;The third and fourth X on behalf of the date, 01-31 said; The last two X represents the wafer batch code.

➢ Absolute Maximum Ratings (Note 1)

Parameter	Value	Unit
VDD DC Supply Voltage	30	V
VDD DC Clamp Current	10	mA
Drain Pin	-0.3 to 650	V
FB, CS Voltage Range	-0.3 to 7	V
Package Thermal Resistance---Junction to Ambient(DIP-8)	80	℃/W
Maximum Junction Temperature	175	℃
Storage Temperature Range	-65 to 150	℃
Lead Temperature (Soldering, 10sec.)	260	℃
ESD Capability, HBM (Human Body Model)	4	kV
ESD Capability, MM (Machine Model)	500	V

Note1. Stresses listed as the above "Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to maximum rating conditions for extended periods may remain possibility to affect device reliability.

BLOCK DIAGRAM



RECOMMENDED OPERATION CONDITIONS (Note 2)

Parameter	Value	Unit
Supply Voltage, VDD	10 to 26	V
OPERATING AMBIENT TEMPERATURE	-40 TO 85	℃

ELECTRICAL CHARACTERISTICS (Ta = 25°C, VIN=12V, if not otherwise noted)

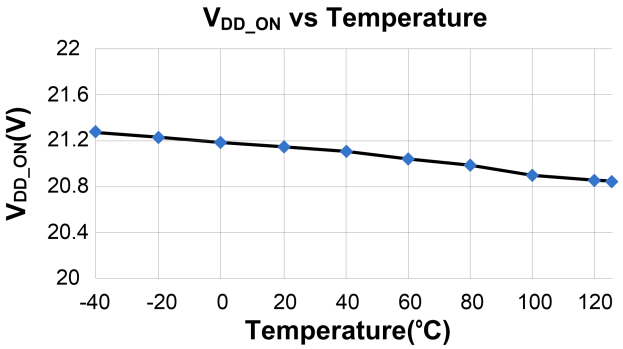
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
Supply Voltage Section(VDD Pin)						
I_{VDD_st}	Start-up current into VDD pin			2	20	uA
I_{VDD_Op}	Operation Current	V_{FB}=3V		1.2	2	mA
$I_{VDD\_standby}$	Standby Current			0.6	1	mA
V_{DD_ON}	VDD Under Voltage Lockout Exit		19	21	22.5	V
V_{DD_OFF}	VDD Under Voltage Lockout Enter		8	9	10	V
V_{DD_OVP}	VDD OVP Threshold		29	31	33	V
V_{DD_Clamp}	VDD Zener Clamp Voltage	$I(V_{DD})$=7 mA	33	35	37	V
Feedback Input Section (FB Pin)						
V_{FB_Open}	FB Open Voltage			5.9		V
I_{FB_Short}	FB Short Circuit Current	Short FB Pin to GND, Measure Current		0.3		mA
Z_{FB_IN}	FB Input Impedance			20		KΩ
A_{CS}	PWM Gain	$\Delta V_{FB}/\Delta V_{CS}$		2.0		V/V
V_{skip}	FB Under Voltage PWM Clock is OFF			1.0		V
V_{TH_OLP}	Power Limiting FB Threshold Voltage			3.6		V
T_{D_OLP}	Power Limiting Debounce Time	SEL Pin is floating		75		ms
Current Sense Input Section (CS Pin)						
T_{LEB}	CS Input Leading Edge Blanking Time			250		ns
$V_{cs(max)}$	Current limiting threshold		0.97	1.0	1.03	V
T_{D_OC}	Over Current Detection and			70		ns

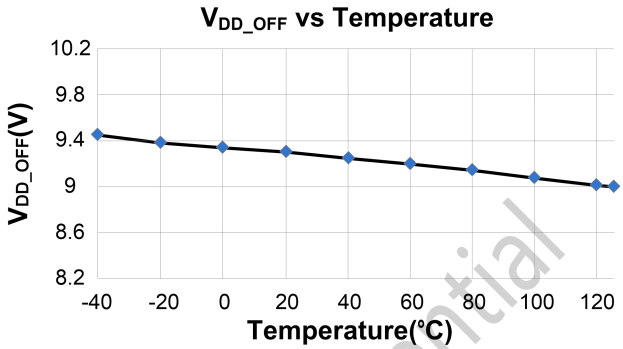
	Control Delay					
Oscillator Section						
F_{OSC}	Normal Oscillation Frequency		60	65	70	KHz
$\Delta F(shuffle)/F_{OSC}$	Frequency Shuffling Range		-4		4	%
T(shuffle)	Frequency Shuffling Period			32		ms
D_{MAX}	Maximum Switching Duty Cycle			66.7		%
F_{Bust}	Burst Mode Base Frequency			22		KHz
On-Chip Thermal Shutdown						
T_{SD}	Thermal Shutdown	(Note 3)	---	165	--	℃
T_{RC}	Thermal Recovery	(Note 3)		140	--	℃
Power MOSFET Section (Drain Pin)						
V_{BR}	Power MOSFET Drain Source Breakdown Voltage		650			V
R_{dson}	Static Drain-Source On Resistance			0.9		Ω
I_D	Drain current			4.5		A

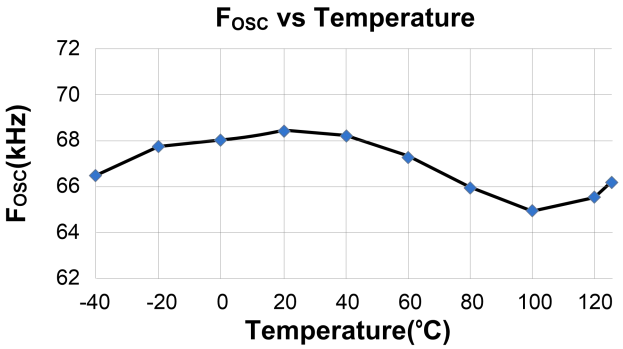
Note2. The device is not guaranteed to function outside its operating conditions.

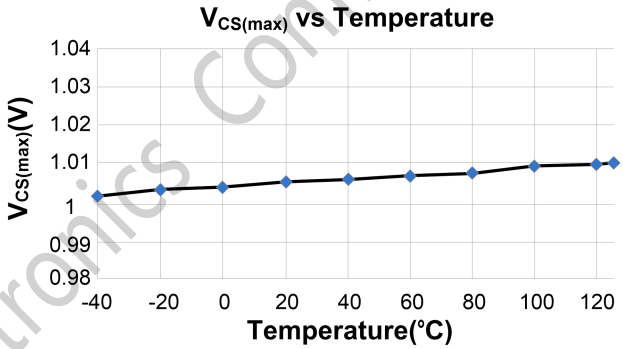
Note3. Guaranteed by the Design.

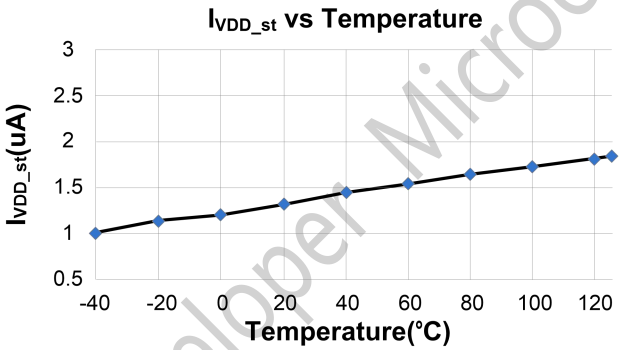
CHARACTERIZATION PLOTS











OPERATION DESCRIPTION

DP2363 is a high performance current mode PWM power switch for offline flyback converter, motor driver power supply, and adapter applications.

- **System Start-Up Operation and IC Operation Current**

Before the IC starts to work, it consumes only startup current (typically 2uA) which allows a large value startup resistor to be used to minimize the power loss and the current flowing through the startup resistor charges the VDD hold-up capacitor from the high voltage DC bus. When VDD reaches turn on threshold VDD_ON (typical 21V), DP2363 begins switching and the IC operation current is increased to be 1.2mA (typical). The hold-up capacitor continues to supply VDD before the auxiliary winding of the transformer takes the control of VDD voltage. When the IC enters into burst mode, the IC operation current will decrease further, thus less than 75mW standby power.

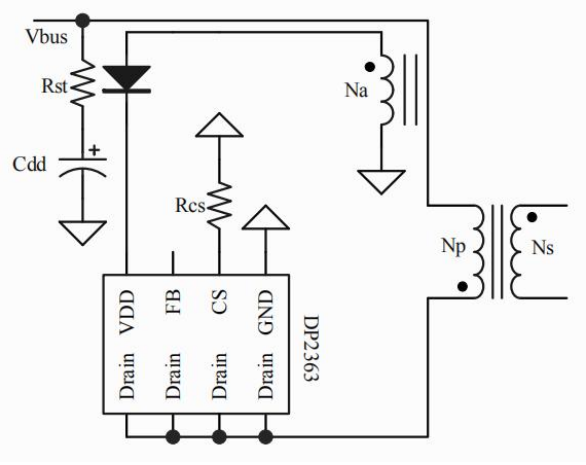


Fig.1

- **Oscillator with Frequency Shuffling**

PWM switching frequency in DP2363 is fixed to 65KHz and is trimmed to tight range. To improve system EMI performance, DP2363 operates the system with 4% frequency shuffling around setting frequency.

- **Green Mode Operation**

Since the main power dissipation at light/zero load in a switching mode power supply is from the switching loss which is proportional to the PWM switching frequency. To meet green mode requirement, it is necessary to reduce the switching cycles under such conditions either by skipping some switching pulses or by reducing the switching frequency.

- **Smooth Frequency Foldback**

In DP2363, a Proprietary "Smooth Frequency Foldback" function is integrated to foldback the PWM switching frequency when the loading is light. Compared to the other frequency reduction implementations, this technique can reduce the PWM frequency smoothly without audible noise.

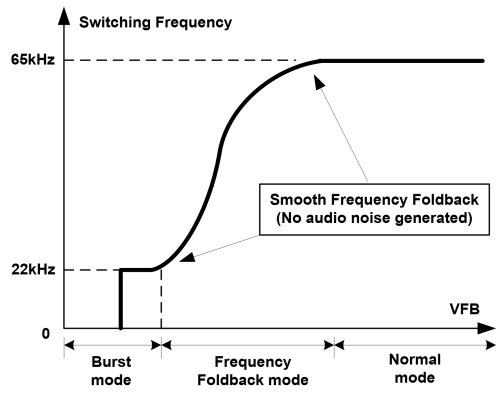


Fig.2

- **Burst Mode Control**

When the loading is very small, the system

enters into burst mode. When VFB drops below Vskip, DP2363 will stop switching and output voltage starts to drop (as shown in Fig.3), which causes the VFB to rise. Once VFB rises above Vskip, switching resumes. Burst mode control alternately enables and disables switching, thereby reducing switching loss in standby mode.

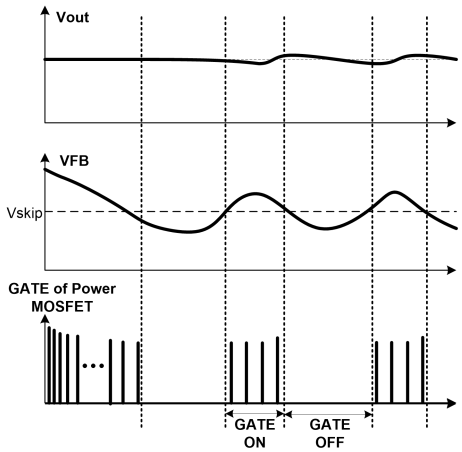


Fig.3

- **Built-in Slope Compensation**

In the conventional application, the problem of the stability is a critical issue for current mode controlling, when it operates in higher than 50% of the duty-cycle. In DP2363 the slope compensation circuit is integrated by adding voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

- **Leading Edge Blanking (LEB)**

Each time the power MOSFET is switched on, a turn-on spike occurs across the sensing resistor. The spike is caused by primary side capacitance and secondary side rectifier reverse recovery. To avoid premature termination of the switching pulse, an internal leading edge blanking circuit is built in. During this blanking period (250ns, typical), the PWM comparator is disabled and cannot switch off the gate driver.

- **On Chip Thermal Shutdown (OTP)**

When the IC temperature is over 165 °C, the IC shuts down. Only when the IC temperature drops to 140 °C, IC will restart.

- **Soft Start**

DP2363 features an internal 2ms (typical) soft start that slowly increases the threshold of cycle-by-cycle current limiting comparator during startup sequence. It helps to prevent transformer saturation and reduce the stress on the secondary diode during startup. Every restart attempt is followed by a soft start activation.

- **Constant Power Limiting**

A proprietary "Constant Power Limiting" block is integrated to achieve constant maximum output power capability over universal AC input range. Based on the duty cycle information, the IC generates OCP threshold according to a proprietary analog algorithm.

- **Over Load Protection (OLP)**

If over load occurs, a fault is detected. If this fault is present for more than 75ms (typical), the protection will be triggered, the IC will experience an auto-recovery mode protection as mentioned above. The 75ms delay time is to prevent the false trigger from the power-on and turn-off transient.

- **VDD Over Voltage Protection (OVP) and Zener Clamp**

When VDD voltage is higher than 31V (typical), the IC will stop switching. This will cause VDD fall down to be lower than V_{DD_OFF} (typical 9V) and

then the system will restart up again. An internal 35V (typical) zener clamp is integrated to prevent the IC from damage.

- **CS Pin Float Protection**

When VDD voltage is higher than V_{DD_ON} (21V typical), IC firstly starts to check whether CS pin is floated. If CS pin is floated, switching is blocked and IC enters auto-recovery mode; otherwise, normal work begins. With this protection, system stability is enhanced.

- **Auto Recovery Mode Protection**

As shown in Fig.4, once a fault condition is detected, PWM switching will stop. This will cause VDD to fall because no power is delivered form the auxiliary winding. When VDD falls to V_{DD_OFF} (typical 9V), the protection is reset and the operating current reduces to the startup current, which causes VDD to rise. The system begins switching when VDD reaches to V_{DD_ON} (typical 21V). However, if the fault still exists, the system will experience the above mentioned process. If the fault has gone, the system resumes normal operation. In this manner, the auto restart can alternatively enable and disable the switching until the fault condition is disappeared.

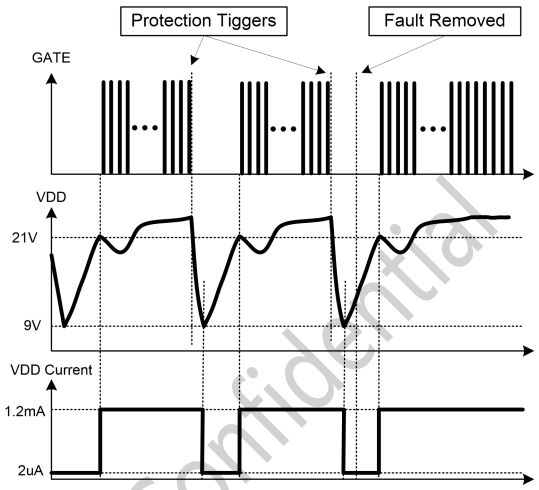


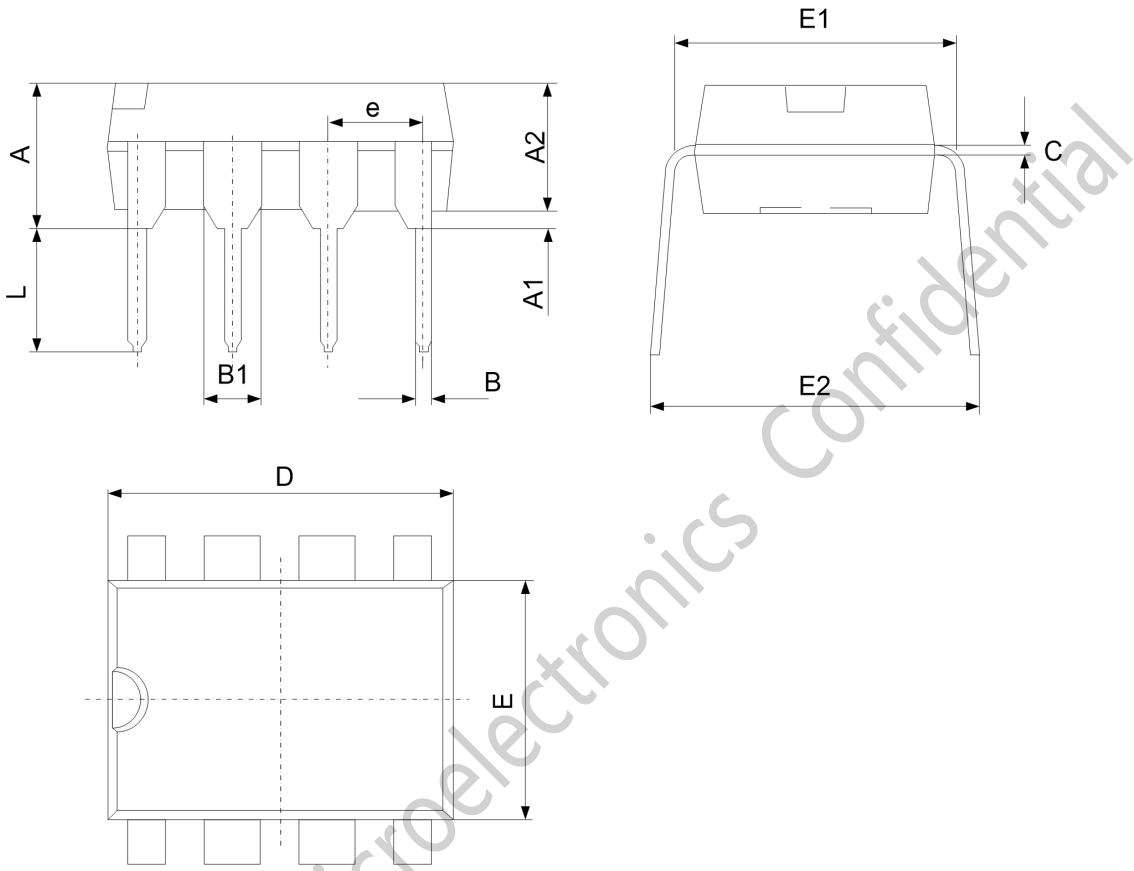
Fig.4

- **Soft Totem-Pole Gate Driver**

DP2363 has a soft totem-pole gate driver with optimized EMI performance. An internal gate clamp is added for power MOSFET gate protection when high VDD input.

PACKAGE DIMENSION

DIP8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524 (BSC)		0.06 (BSC)	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.100 (BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

OFFICIAL ANNOUNCEMENT

Division I will ensure the accuracy and reliability of the product specification document, but we reserve the right to independently modify the content of the specification document without prior notice to the customer. Before placing an order, customers should contact us to obtain the latest relevant information and verify that this information is complete and up-to-date. All product sales are subject to the sales terms and conditions provided by our company at the time of order confirmation.

Division I will periodically update the content of this document. Actual product parameters may vary due to differences in models or other factors. This document does not serve as any express or implied guarantee or authorization.

The product specification does not include any authorization for the intellectual property owned by our company or any third party. With respect to the information contained in this product specification, we make no explicit or implied warranties, including but not limited to the accuracy of the specification, its fitness for commercial use, suitability for specific purposes, or non-infringement of our company's or any third party's intellectual property. We also do not assume any responsibility for any incidental or consequential losses related to this specification document and its use.

We do not assume any obligations regarding application assistance or customer product design. Customers are responsible for their own use of our company's products and applications. In order to minimize risks associated with customer products and applications, customers should provide thorough design and operational safety validation.

The reproduction, transmission or use of this document or its contents is not permitted without express written authority. Once discovered, the company will pursue its legal responsibility according to law and compensate for all losses caused to the company.

Please note that the product is used within the conditions described in this document, paying particular attention to the absolute maximum rating, operating voltage range, and electrical characteristics. The Company shall not be liable for any damage caused by malfunctions, accidents, etc. caused by the use of the product outside the conditions stated in this document.

Division I has been committed to improving the quality and reliability of products, but all semiconductor products have a certain probability of failure, which may lead to some personal accidents, fire accidents, etc.When designing products, pay full attention to redundancy design and adopt safety indicators, so as to avoid accidents.

When using our chips to produce products, Division I shall not be liable for any patent dispute arising from the use of the chip in the product, the specification of the product, or the country of import, etc., in the event of a patent dispute over the products including the chip.