

## Non-isolated Quasi-Resonant Buck LED Power Switch

### **FEATURES**

- Integrated with 500V MOSFET
- Integrated HV VDD Power Supply Circuit
- No VDD Cap Design
- ±5% CC Regulation
- Quasi-Resonant for High Efficiency
- Very Low VDD Operation Current
- Built-in AC Line CC Compensation
- Build in Protections:
- Cycle-by-Cycle Current Limiting
- Leading Edge Blanking (LEB)
- LED Short/Open Protection
- On-Chip Thermal Fold-back (OTP)

## **APPLICATIONS**

High Power LED Lighting

### GENERAL DESCRIPTION

DP951X is a highly integrated power switch with Quasi-Resonant Buck (QR-Buck) constant current (CC) control for LED lighting applications without auxiliary winding.

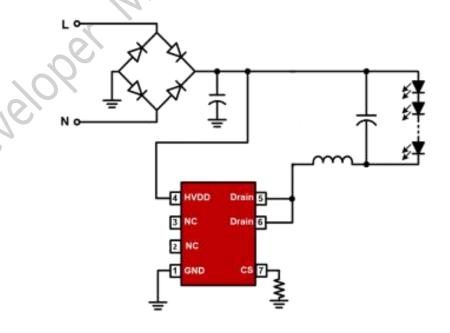
DP951Xcombines a 500V power MOSFET and high voltage startup/IC supply circuit in one chip which reduced system design cost. The IC also adopts high accuracy current sensing control method which maintains accurate output current and good line/load regulation.

DP951X integrates functions and protections of Current Limit and Leading-Edge Blanking, Under Voltage Lockout (UVLO), Cycle-by-cycle Current Limiting (OCP), Thermal Foldback (OTP),,LED Open/Short Protection, etc.

## ORDERING INFORMATION

Part Number	Description				
DP951X	SOP-7, halogen free 4000pcs/reel				

## TYPICAL APPLICATION CIRCUIT



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## PRODUCT DESCRIPTION

## > Pin Configuration



## > Pin Description

Pin Number	Pin Name	Description
1	GND	IC Ground
2,3	NC	No Function Pin and Left Floating in Application
4	HVDD	IC HV Supply Pin
5,6	Drain	Internal Power MOSFET Drain Terminal
7	CS	Internal Power MOSFET Source Terminal and Current Sensing Input Pin

## > Marking Information



#### DP951X for product name:

XXXXXX The first X represents the last year,2014 is 4;The second X represents the month,inA-L 12 letters;The third and fourth X on behalf of the date,01-31said;The last two X represents the wafer batch code

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## Output Power Table

Part Number	Package	Output Current for 176-264Vac		Minimum Output	
	-	36V output	72V output	Voltage	
DP9511L		100 mA	80 mA		
DP9511M		130 mA	120 mA		
DP9511S	COD 7	180 mA	150 mA	2011	
DP9511A	SOP-7	220 mA	180 mA	30V	
DP9511		260 mA	230 mA		
DP9512		300 mA	280 mA	76,	

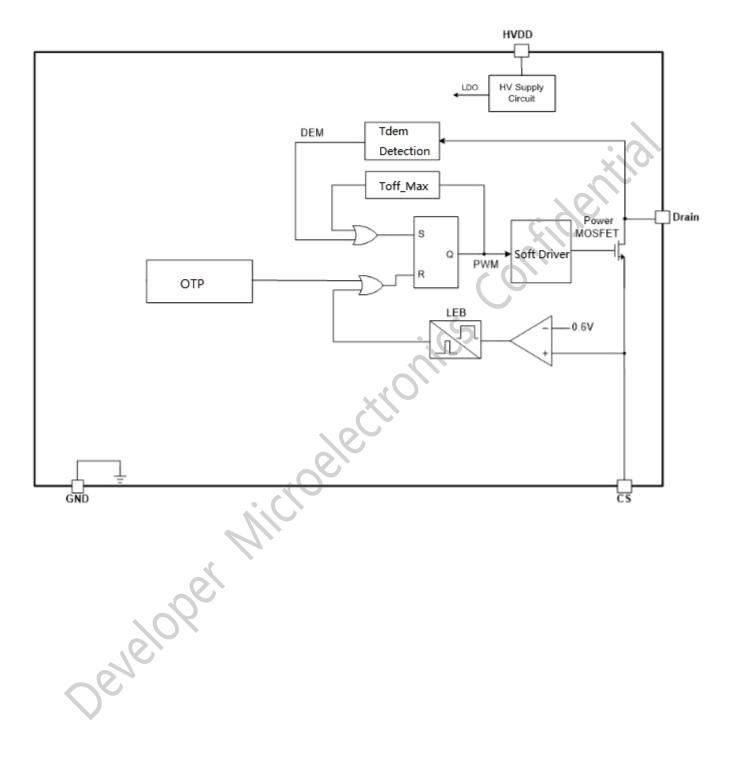
# ➤ Absolute Maximum Ratings(Note 1)

Parameter	Value	Unit
Drain Voltage	-0.3 to 500	V
HVDD Voltage	-0.3 to 650	V
CS,ROVP Voltage	-0.3 to 7	V
P <sub>Dmax</sub> , Power dissipation @T <sub>A</sub> =50°C (SOP-7) (Note 2)	0.6	W
$\theta_{JA}$ , Thermal ResistanceJunction to Ambient (SOP-7)	165	°C/W
IC Junction Temperature	150	°C
Storage Temperature Range	-65 to 150	°C
Lead Temperature (Soldering, 10sec.)	260	°C
ESD Capability, HBM (Human Body Model)	3	kV

**Note1.** Stresses listed as the above "Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to maximum rating conditions for extended periods may remain possibility to affect device reliability.



## **BLOCK DIAGRAM**





## **RECOMMENDED OPERATION CONDITIONS**

Parameter	Value	Unit
Operating Junction Temperature	-40 to 125	°C

## **ELECTRICAL CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Min	Тур.	Max	Unit
Supply Volta	age Section(HVDD Pin)		•	16/		
$I_{VDD\_st}$	Startup Current	VDD <v<sub>DD_Op</v<sub>		300	700	uA
$I_{VDD\_Op}$	Operation Current	Fsw=7KHz	80	150	300	uA
$HV_{DD\_ON}$	HVDD Pin Startup Voltage		10	11.5	13	V
$HV_{DD\_OFF}$	HVDD Pin Lockout Voltage	.(5	5.8	6.6	7.5	V
$T_{off\_min}$	Minimum Off Time	(Note 3)	0.6	1.0	1.4	us
T <sub>on_max</sub>	Maximum On Time	(Note 3)		50		us
$T_{off\_max}$	Maximum Off Time	6	195	270	350	us
Current Sen	se Input Section (CS Pin)					
$T_{LEB}$	CS Input Leading Edge Blanking Time	(Note 3)	300	500	700	ns
$V_{cs(max)}$	Current limiting threshold		590	600	610	mV
$T_{D\_OC}$	Over Current Detection and Control Delay	(Note 3)		100		ns
Over Tempe	rature Protection(OTP Pin)					
T <sub>SD</sub>	Thermal Shutdown Trigger Point	(Note 3)		140		°C
HV Startup	and Power Supply Section (Drain P	in)	1	1		
I <sub>HV</sub>	HV Charging Current	Drain =20V		6		mA
I <sub>HV_leak</sub>	HV Leakage Current		10	40	60	uA
Power MOS	FET Section (Drain Pin)	1	1	1		

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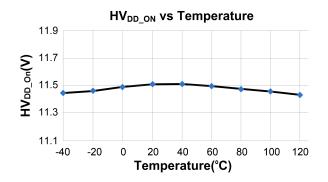
### Non-isolated Quasi-Resonant Buck LED Power Switch

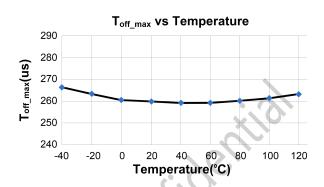
$V_{BR}$	Power MOSFET Drain Source Breakdown Voltage		500			V	
		DP9511L		26		Ω	
		DP9511M		22		Ω	
D.	Static Drain-Source On	DP9511S		16		Ω	
R <sub>dson</sub>	Resistance	DP9511A		12		Ω	
		DP9511		8.5	3	Ω	
		DP9512		5		Ω	
	Note2. Maximum Power dissipation P <sub>Dmax</sub> = (T <sub>Jmax</sub> -T <sub>A</sub> )/θ <sub>JA</sub> . As ambient temperature rises, P <sub>Dmax</sub> will decrease.  Note 3. Guaranteed by the Design.						

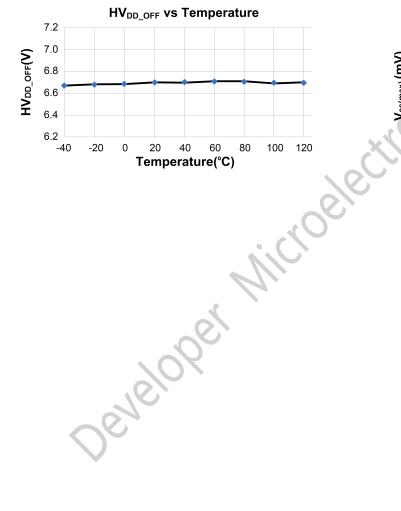
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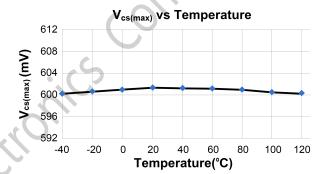


## **CHARACTERIZATION PLOTS**









## **OPERATION DESCRIPTION**

DP951Xcombines a high voltage power MOSFET switch with a power controller in one chip. The built-in high precision CC control with high level protection features makes it suitable for LED lighting applications.

### • HVDD Supply

DP951X integrates 650V high voltage power supply circuit by which the gate drive of the power MOSFET is directly powered without external VDD capacitor.

#### Constant Current Control

In QR-Buck mode, the IC keeps CS peak current constant and starts new PWM cycle with valley switching. Therefore, high precision CC and high conversion efficiency can be achieved simultaneously. The average LED regulation output current is given by:

$$I_{\text{CC\_OUT}}\left(mA\right) = \frac{1}{2} \bullet \frac{V_{\text{cs(max)}}}{R_{\text{cs}}} = \frac{300 mV}{R_{\text{cs}}\left(\Omega\right)}$$

In the equation above,

Rcs--- the sensing resistor connected between the CS pin to IC GND.

### Current Limit and Leading Edge Blanking

The current limit circuit samples the differential voltage between GND and CS Pin. When the. An internal leading edge blanking circuit is built in. During this blanking period (500ns, typical), the cycle-by-cycle current limiting comparator is disabled and cannot switch off the GATE driver.

#### Demagnetization Detection

In DP951X, the demagnetization detection circuit is designed internally without auxiliary winding, which reduces system design cost.

#### Minimum and Maximum OFF Time

In DP951X, a minimum OFF time (typically 1us) is implemented to suppress ringing when the power MOSFET is off. The maximum OFF time in DP951X is typically 270us.

#### On Chip Thermal Fold-back (OTP)

DP951X integrates thermal fold-back function. When the IC temperature is over 140 °C, the system output regulation current is gradually reduced, as shown in Fig.1.Thus, the output power and thermal dissipation are also reduced. In this way, the system temperature is limited and system reliability is also improved.

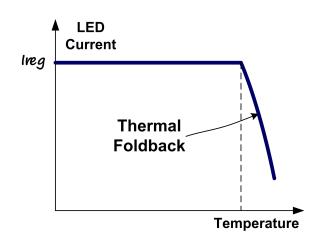


Fig.1

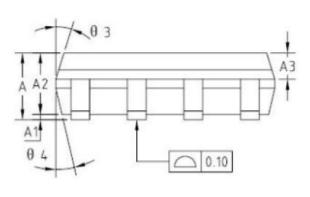
#### • Soft Totem-Pole Gate Driver

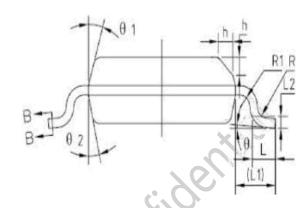
DP951X has a soft totem-pole gate driver with optimized EMI performance.

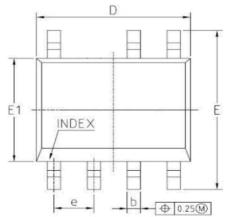


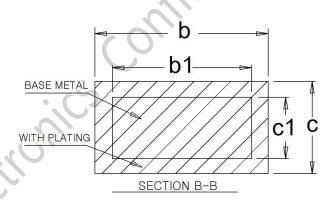
## **PACKAGE DIMENSION**

SOP-7









Symbol	Dimensions in Millimeters					
Symbol	Min	Nom	Max			
Α	1.45	1.55	1.65			
A1	0.10	0.15	0.20			
A2	1.353	1.40	1.453			
A3	0.55	0.60	0.65			
b	0.38	-	0.51			
b1	0.37	0.42	0.47			
С	0.17	-	0.25			
c1	0.17	0.20	0.23			
D	4.85	4.90	4.95			
E	5.85	6.00	6.15			
E1	3.85	3.90	3.95			
е	1.245	1.27	1.295			
L	0.45	0.60	0.75			
L1	-	1.050REF	-			
L2	-	0.250BSC	-			
Θ1-Θ4		12° REF				
h		0.40REF				
R		0.15° REF				
R1		0.15° REF				

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