LED Co negative driving IC

1 Overview

DP32029C is a serial decoding common cathode driver chip designed specifically for LED scanning screens. Integrated 8-channel NMOS row switch circuit, with high-performance adaptive shadow cancellation, LED bead short circuit and open circuit series lighting processing functions. Integrating a serial decoding circuit that prevents multiple channels from simultaneously opening can prevent the burning of the chip due to excessive channel current caused by the simultaneous opening of three or more channels. DP32029C can completely replace the original 3-8 decoder (74HC138) circuit of LED modules, effectively simplifying the complexity of LED module PCB wiring and improving the overall image effect of the display screen.

2 Characteristics

- working voltage 3.0V~5 .5V
- Integrated to prevent multi-channel simultaneous activation of serial decoding circuit
- Support arbitrary scanning
- Integrated 8-channel power NMOS transistor
  - OUT_MAX = 2.5A @ VDD = 5.0V
  - RON=80mΩ@VDD=5.0V&IOUT=1.0A
- Maximum power consumption< 600 mW @ VDD = 5.0V
- Integrated anti ghosting adaptive function, effectively eliminating line dragging shadows
- The erasing potential can be configured with registers to adapt to more complex environments
- Improve the display cross line phenomenon caused by LED open circuit
- Simplify the complexity of LED module PCB wiring
- Packaging form:SOP16，QFN4*4-16L
- Excellent ESD characteristics

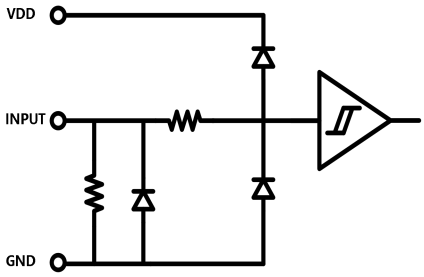
3 Application areas

- High refresh rate LED video display
- Single color dual color full-color LED display
- High density and small spacing LED light board display

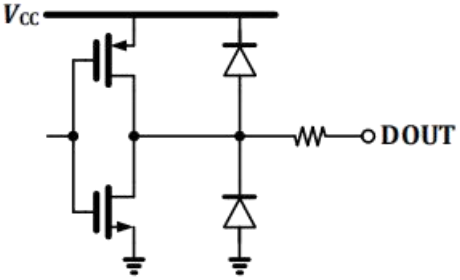
4 Circuit schematic diagram

4.1 Internal Circuit Block Diagram

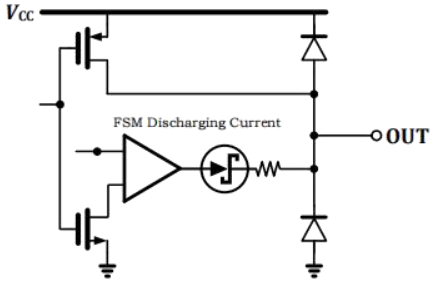
SDI,LATCH,SCK Input terminal



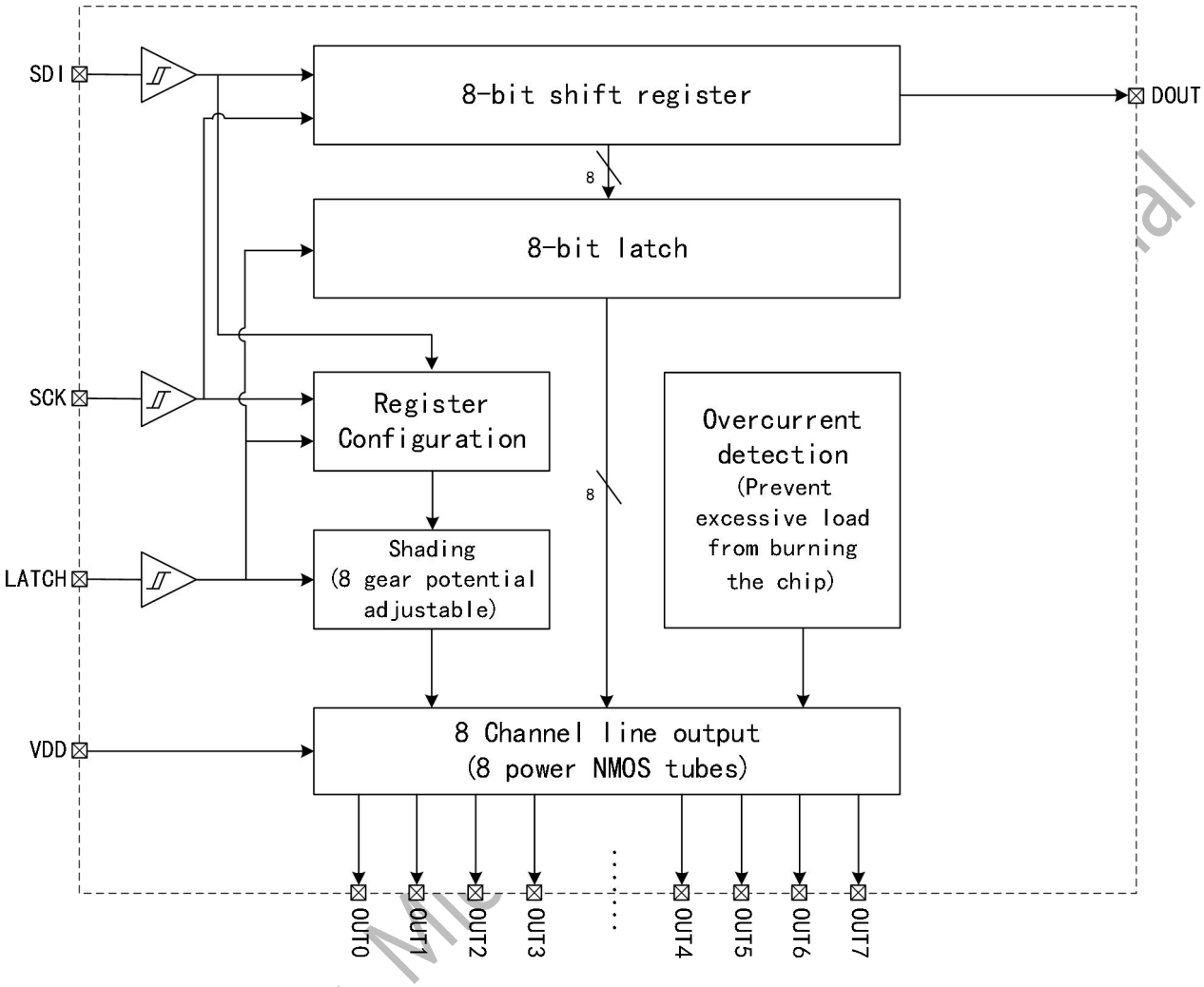
DOUT Output terminal



OUT0~7 Output terminal



4.2 Internal Circuit Block Diagram



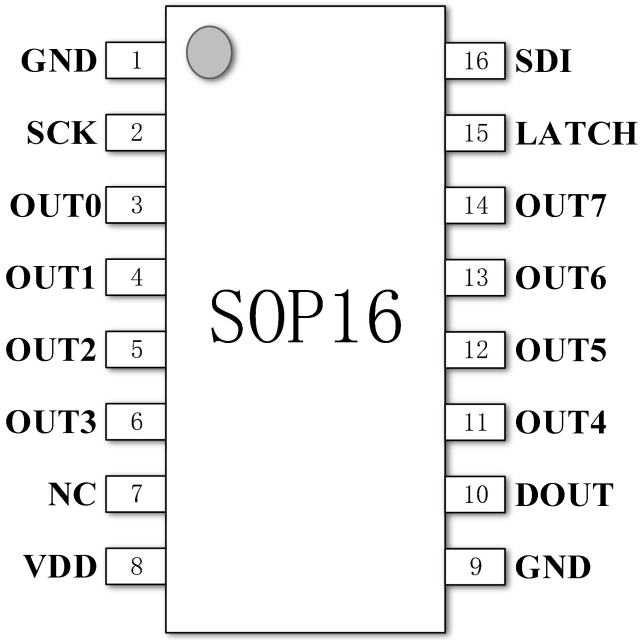
Directory

Revision History

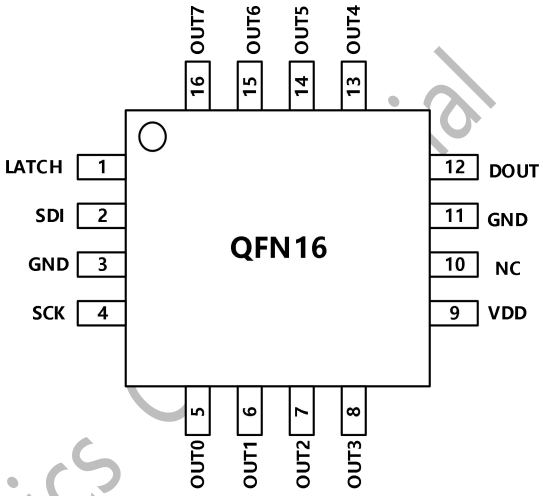
version	Revision date	Revised by	Revision content
V1.0	2023.12	WM	1.Initial version
V1.1	2024.03	WM	1. Modify the number of scans supported 2. Modify the equivalent circuit of input and output
V1.2	2025.02	WM	1. Modify the QFN4*4-16L Package information
V1.3	2025.03	WM	1. Modify Row switch control 2. Modify the configuration register
V1.4	2025.04	WM	1. Modify the Package information

5 Product Description

- Pin definition



SOP16 Pin Definition Diagram



QFN4*4-16L Pin Definition Diagram

- Pin description

SOP16 Pin number	QFN4*4-16L Pin number	Pin Name	pinouts
8	9	VDD	power input
16	2	SDI	data input
15	1	LATCH	Serial signal clock input
2	4	SCK	Configure clock input for blanking register configuration
3~6，4~7	5~8，13~16	OUT0~OUT7	OUT output
1,9	11	GND	grounds
10	12	DOUT	serial data output
7	10	NC	Empty foot

- Product ordering information

product name	Packaging form	Packaging method	Quantity/Plate	Humidity sensitivity level
DP32029C	SOP16	braid	4000	MSL=3
	QFN4*4-16L	braid	5000	

- Product labeling

SOP16

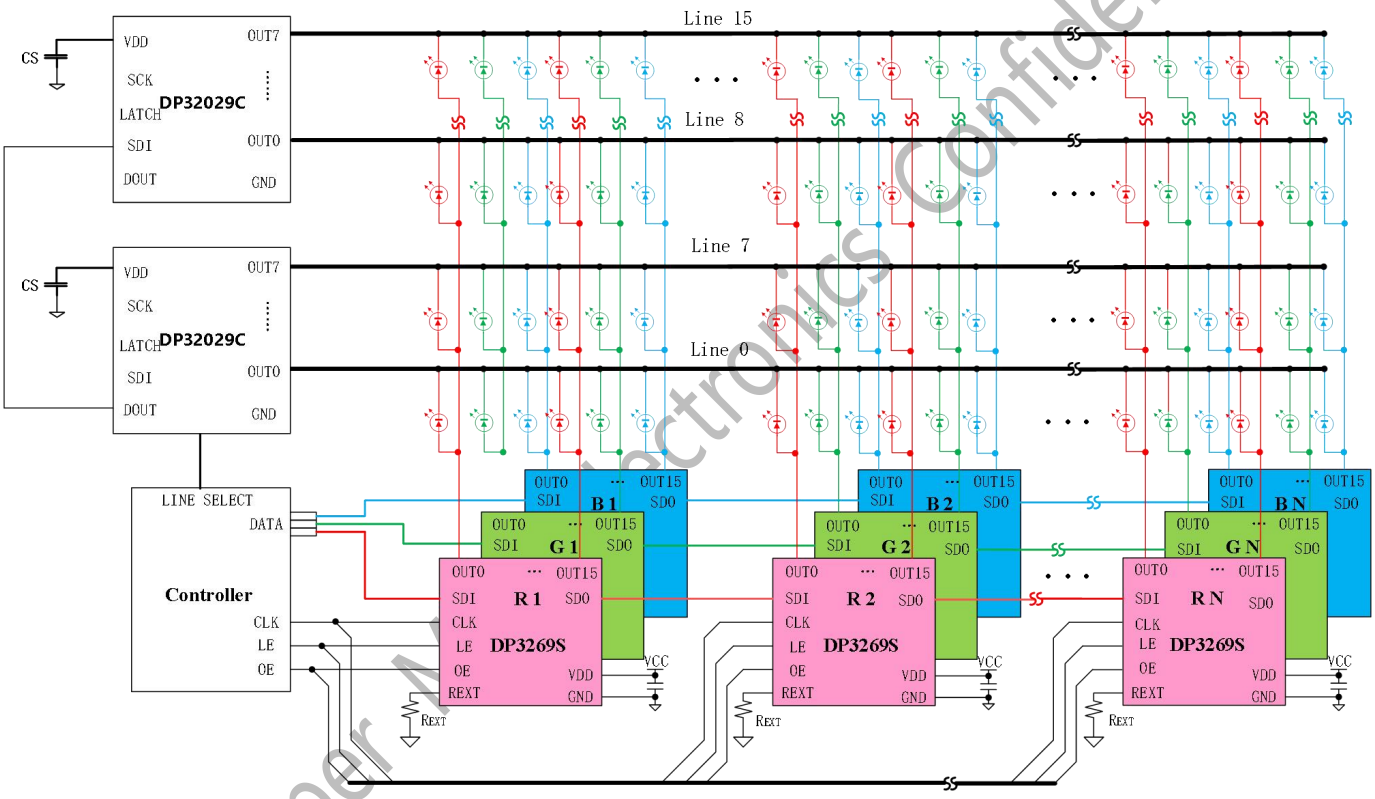
QFN4*4-16L

DP32029C is the product name
XXXXXX represents the product batch number

6 Suggestions for Applying Circuits

Due to the widespread use of LED scanning screens in indoor display screens to reduce costs, the parasitic capacitance of the LED anode can instantly generate a discharge path during scanning switching, causing the display screen to experience ghosting; Users can use the DP32029C with discharge circuit function and refer to the recommended application circuit for the scanning screen shown in the figure below, and pair it with the built-in constant current driver chip DP5125 with pre charging function, which can completely eliminate the up and down ghosting phenomenon.

Due to the fact that DP32029C is an 8-channel output integrated power chip, to avoid excessive heat accumulation, it is recommended to use it on display screens with 16 or more scans, and pay attention to the temperature conditions during use.



LED Display Screen 16 Scan Application Block Diagram

7 Parameter Table

7.1 Maximum limit parameters

project	symbol	Rated Value	unit
supply voltage	V_{CC}	0~6.0	V
Input voltage (all pins)	V_{IN}	-0.4~V_{DD}+0.4	V
Continuous working current at OUT end	I_D	-2.5	A
Instantaneous maximum current at OUT end	I_{OUT_MAX}	-3.5	A
power loss	PD	<600	mW
Encapsulation thermal resistance	$R_{th(j-a)}$	80	℃/W
operation temperature	T_{opr}	-40~85	℃
storage temperature	T_{stg}	-40~150	℃
HBM Human Body Model	V_{ESD}	≥8	KV

- All voltage values are based on the chip ground terminal (GND) as the reference point, and the maximum limit parameter test temperature is 25 ℃.
- If the actual working conditions exceed the specified values, it may cause permanent damage to the components; If the actual working conditions are slightly lower than the maximum value and work for a long time, it may reduce the reliability of the components. The above are only partial specified values, and this product does not support functional operations under conditions other than specifications.
- The maximum peak welding temperature of surface mounted products cannot exceed 260 ℃, and the temperature curve should be set by the factory according to the J-STD-020 standard, reference to the actual situation of the factory, and recommendations from the solder paste manufacturer.

7.2 Recommended scope of work

project	symbol	Test conditions	minimum value	Typical values	Maximum value	unit
supply voltage	V_{CC}	-	3.5	5.0	5.5	V
Output voltage(DOUT)	V_{DOUT}	-	0.7	-	V_{DD}	V
Output current(DOUT)	I_{OH}	V_{OH} =V_{DD} -0.5V	-	-16	-	mA
	I_{OL}	V_{OL} =0.5V	-	20	-	
input voltage(SDI,LATCH,SCK)	V_{IH}	V_{DD}=3.3V~5.5V	0.7 V_{DD}	-	V_{DD}	V
	V_{IL}		0	-	0.3V_{DD}	

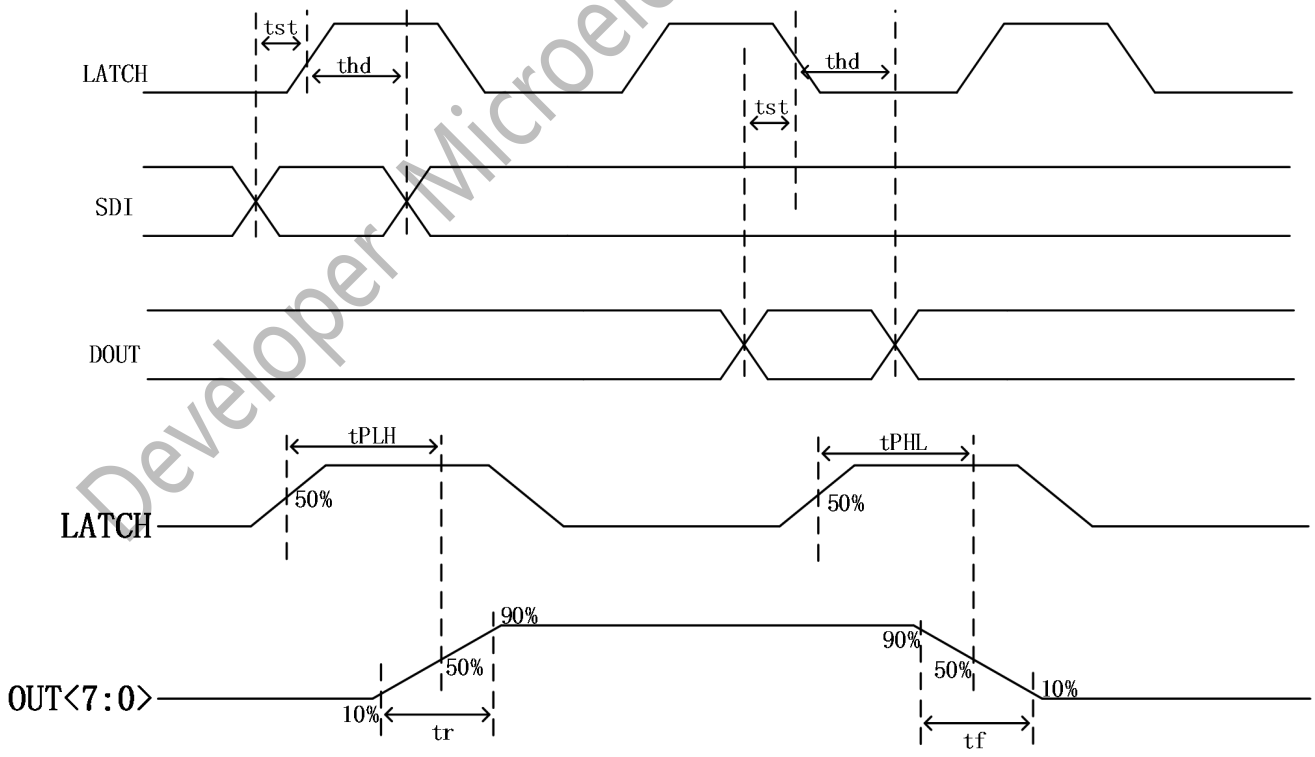
7.3 DC Electrical Characteristics (VDD=5.0V)

project		symbol	Test conditions	minimum value	Typical values	Maximum value	unit
Logic power supply voltage		V_{DD}	-	3.0	5.0	5.5	V
Power supply current		I_{DD_OFF}	All OUT outputs are set to low	-	400	-	uA
Gate opening voltage		$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	-	-0.7	-0.9	V
Source drain conduction resistance		R_{DS}(on)[1:7]	V_{GS}=-5.0V, I_{OUT}=-1.0A	-	80	120	mΩ
input voltage	high level	V_{IH}	Logic potential	0.7 V_{DD}	-	V_{DD}	V
	Low Level	V_{IL}		0	-	0.3 V_{DD}	

7.4 Dynamic Characteristics (Unless otherwise specified, VDD=3.5V~5V, Ta=25 ℃)

project	symbol	Test conditions	minimum value	Typical values	Maximum value	unit
Output rise delay	t_{PLH}	VDD=5.0V CL=12pF	-	50	-	ns
Output descent delay	t_{pHL}		-	100	-	ns
Output rising edge	t_r		-	60	-	ns
Output falling edge	t_f		-	400	-	ns
Establishment time	t_{st}		60	-	-	ns
hold time	t_{hd}		60	-	-	ns

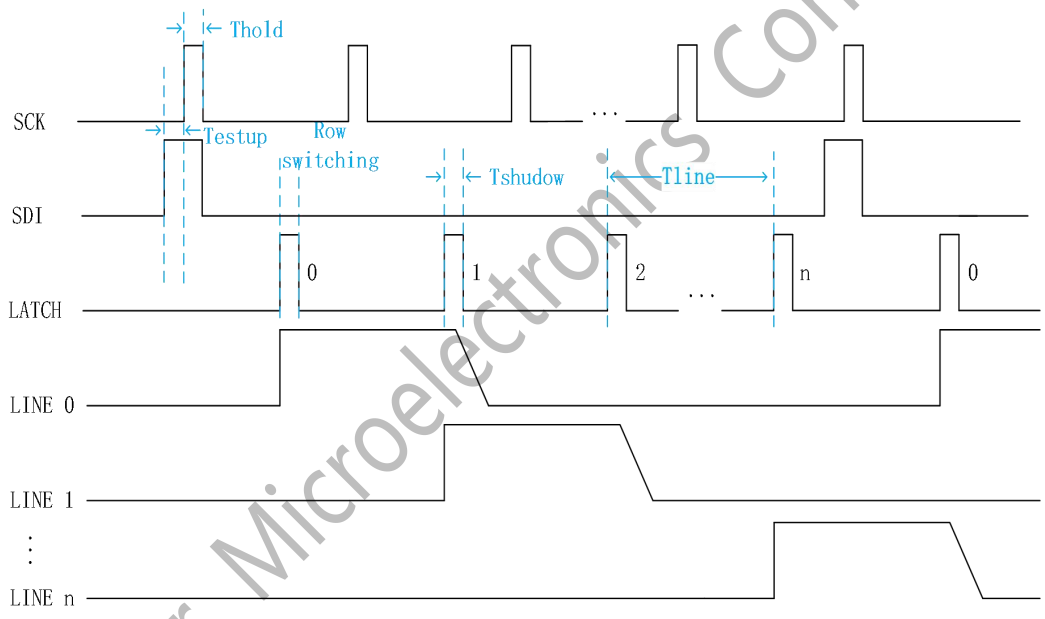
8 Timing waveform diagram



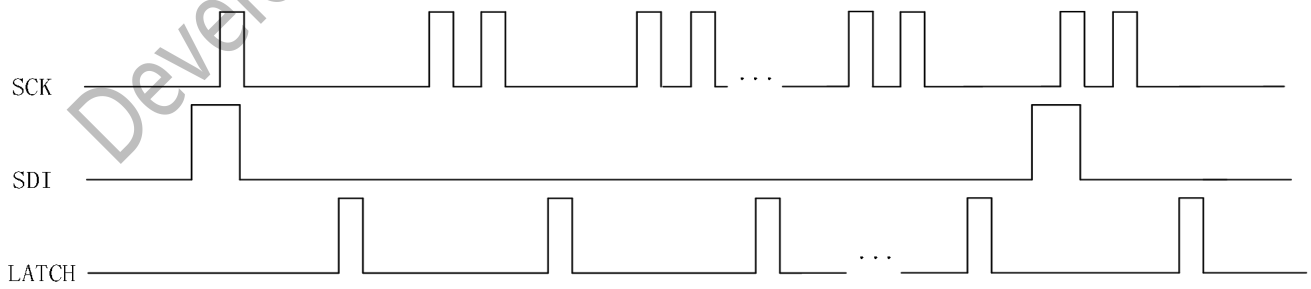
9 Row switch Control and blanking Time

DP32029C is a common cathode display serial decoder line tube driver, where each Row Switch is fixed to send 1 LATCH, and the channel output is high effective; the input data SDI to the output data DOUT is fixed to be at the rising edge interval of 8 SCK.

Symbols	Description	Min value	Max value
Tshadow	Equal to LATCH signal high level width	500ns	-
Tsetup	Setup time	60ns	-
Thold	Hold time	60ns	-

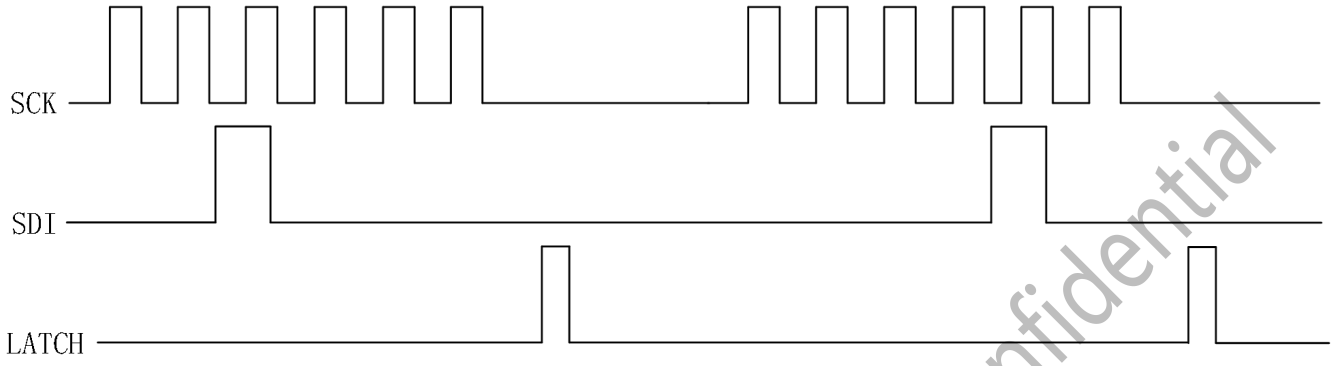


Scan the waveform line by line



Interlaced scanning configuration waveform

Number of rows =6 as an example:
Send 6 SCK impulses，only one SCK rising edge samples to SDI high level，others SCK rising edge is sampled to SDI low level，The time from the back to the front is recorded as the first, the second..6th SCK rising edge.If the NTH SCK rising edge is sampled to the SDI high level, Step 2 enable the display of the NTH channel.



Configuration waveform for any scan

10 Configuration register

DP32029C Built in 4bit register:

BIT	Name	Default	Description		
3	VR_UP[2]	1’ b1	Pull up the erasing circuit reference potential configuration register ,the highest bit in VR_UP[2:0]		
2	reserved	1’ b0	reserved		
1:0	VR_UP[1:0]	2’ b10	Pull up the cancellation circuit reference potential according to the register, VR_UP[2:0] can be set to (Vdd=5V)-		
			0000：Vdd*7/20 =1.75V 0001：Vdd*8/20 =2.0V 0010：Vdd*9/20 =2.25V 0011：Vdd*10/20 =2.5V	1000：Vdd*11/20 =2.75V 1001：Vdd*12/20 =3.0V 1010：Vdd*13/20 =3.25V 1011：Vdd*15/20 =3.5V	Default 2.75V **Data pin matching:** SDI corresponds to c signal of 3-8 decoding; LATCH corresponds to A signal of 3-8 decoding ; SCK corresponds to B signal of 3-8 decoding;

Symbol	Description	Minimum value	Maximum value
Tsetup1	Setup time	60ns	-
Thold1	Hold time	60ns	-

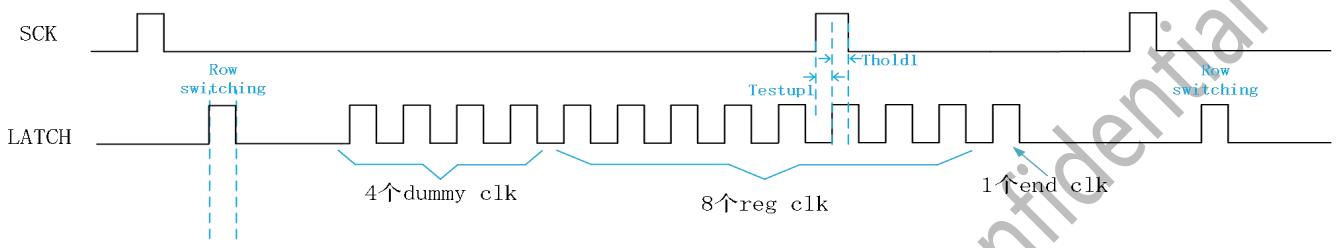
Configuration Register mode:

Register configuration is completed by two signals, SCK and LATCH, the configuration waveform is divided into three steps as shown below:

(1)LATCH sends four dummy CLK pulses, and the chip enters register configuration after receiving them.

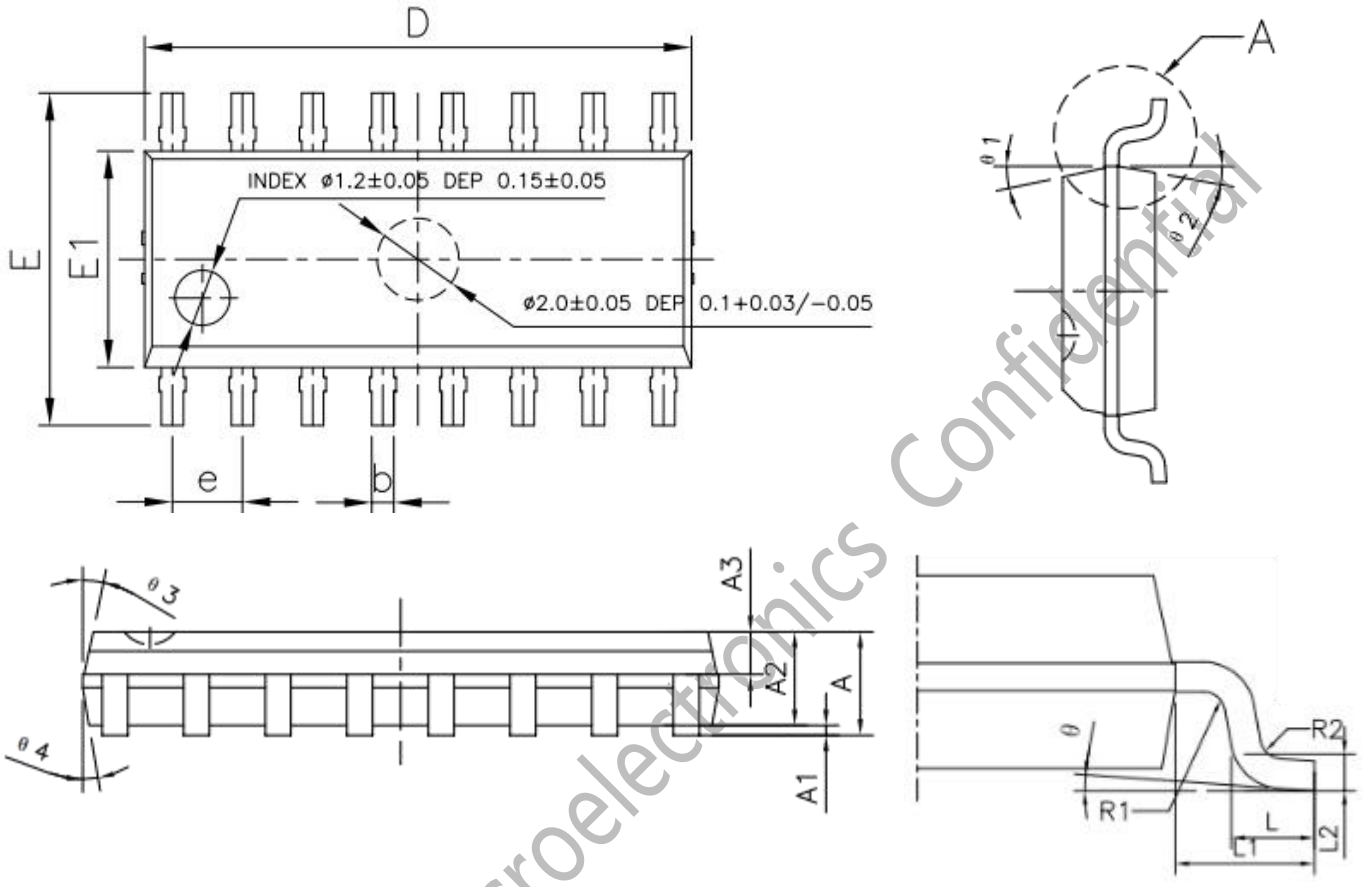
(2)LATCH continues to send 8 CLK pulses, and the value of the sampled SCK of the NTH LATCH pulse is stored in the NTH bit of the register (N=1~8).

(3)LATCH continues to send one CLK pulse, which the chip receives and exits the register configuration state.



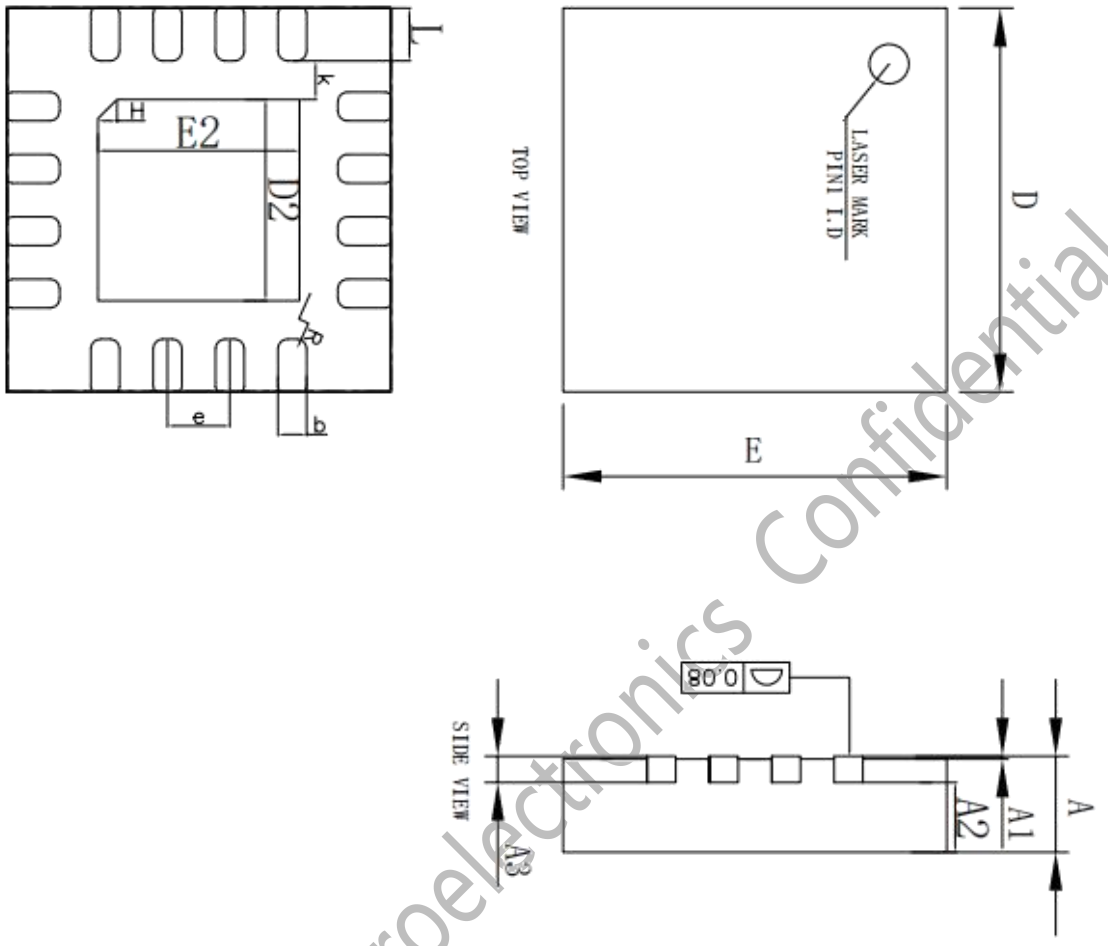
11 Package size

SOP16



Symbol	Min	Nom	Max
A	-	-	1.70
A1	0.10	0.15	0.20
A2	1.42	1.45	1.48
A3	0.62	0.65	0.68
b	0.38	-	0.51
D	9.85	9.90	9.95
E	5.90	6.00	6.10
E1	3.87	3.90	3.93
e	1.24	1.27	1.30
L	0.50	0.60	0.70
L1	1.05REF		
L2	0.25REF		
Θ	0°	-	8°
Θ1-Θ4	12°REF		
R1	0.15REF		
R2	0.15REF		

QFN4*4-16L



Symbol	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.5.	0.55	0.60
A3		0.203REF	
b	0.25	0.30	0.35
D	3.90	4.00	4.10
E	2.90	3.00	3.10
D2	2.00	2.10	2.20
E2	2.00	2.10	2.20
H		0.20REF	
K		0.40REF	
L	0.50	0.55	0.60
e		0.65BSC	
R	0.09		

12 Official Announcement

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