17V, 4A 500KHZ Synchronous Buck Converter

FEATURES

- Up to 95% Efficiency
- Input Voltage Range: 4.5V to 17V
- Output Voltage Range: 0.6V to 7V
- Continuous Output Current: 4A
- CCM Switching Frequency: 500KHz
- Reference Voltage: 0.6V ±2% @25℃
- Integrated MOSFETs: 35mΩ and 15mΩ
- Low Quiescent Current: 200μA
- Low Shutdown Current: 3μA
- COT Control
- Optional Operation Modes at Light-Load Condition:
  - DP31214S: Power Save Mode (PSM)
  - DP31214FS: Continuous Current Mode(CCM)
- Over Current Protection
- Short Protection with Hiccup-Mode
- Internal Soft Startup
- Thermal Shutdown Protection

DESCRIPTIONS

The DP31214S/FS is a low EMI signature, synchronous, step-down, COT-mode converter with internal power MOSFETs. It offers a very compact solution to provide 4.0A continuous current over a wide input supply range, with excellent load and line regulation. DP31214S/FS achieves low EMI signature with well controlled switching edges. Fault condition protection includes programmable -output over-voltage protection, and thermal shutdown. package.

DCM/CCM mode operation provides very low output ripple voltage for noise sensitive applications. Switching frequency is internally. set at 500KHZ, allowing the use of small surface mount inductors and capacitors. Low output voltages are easily supported with the 0.6V feedback reference voltage.

The DP31214S/FS requires a minimal number of readily available, external components and is available in a small package.

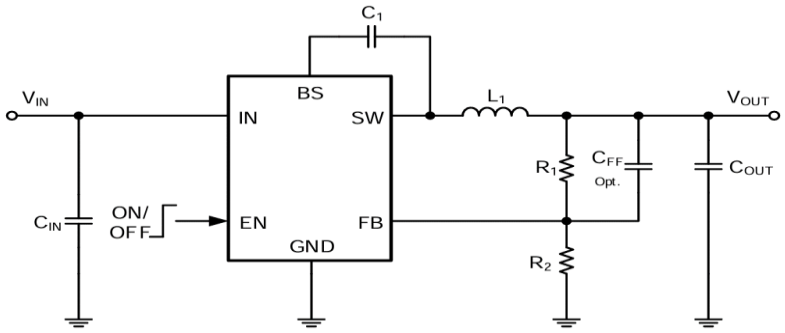
APPLICATIONS

- Automotive Entertainment
- Wireless and DSL Modems
- Digital Set-Top Boxes
- Flat-Panel Television and Monitors
- Digital Still and Video Cameras
- Portable Instruments

ORDERING INFORMATION

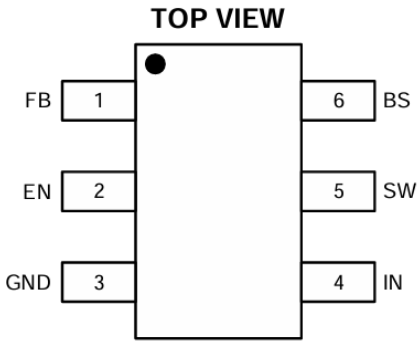
Part Number	Description
TSOT23-6	Pb free in T&R, 3000 Pcs/Reel

TYPICAL APPLICATION CIRCUIT



PRODUCT DESCRIPTION

➢ Pin Arrangement



TSOT23-6

➢ Pin Configuration

TSOT23-6	Pin Name	Description
1	FB	Feedback pin for the internal control loop. Connect this pin to an external feedback divider.
2	EN	Chip Enable Pin. Drive EN above 1.2V to turn on the part. Drive EN below 0.4V to turn it off.
3	GND	Ground Pin
4	IN	Power supply voltage input.
5	SW	Switch pin connected to the internal FET switches and inductor terminal. Connect the inductor of the output filter to this pin.
6	BS	Supply input for the high-side NFET gate drive circuit. Connect a 0.1μF capacitor between VBST and SW pins.

➢ Marking Information

DP31214 for product name:

YYY refers to the following table description, represents different packaging and special functions

XXXX The first X represents the last year,2020 is 0;The second X represents the month,inA-L 12 letters;The third and fourth X on behalf of the date,01-31said;

Marking	Model	Description
31214S	DP31214SST	DP31214SST Buck，4.5V~17V，4.0A，500KHZ，VFB 0.6V，**DCM**，TSOT23-6
31214FS	DP31214FSST	DP31214FSST Buck，4.5V~17V，4.0A，500KHZ，VFB 0.6V，**FCCM**，TSOT23-6

➢ Absolute Maximum Ratings

PARAMETER	Min	Max	Unit
VIN Voltage	-0.3	19	V
EN Voltage	-0.3	19	V
SW Voltage(DC)	-0.3	19	V
SW Voltage(AC less than 10ns while Switching)	-3	21	V
FB Voltage	-0.3	6	V
BS Voltage(vs SW)	-0.3	6	V
Operating junction temperature,TJ	-40	150	℃
Storage temperature, Tstg	-65	150	℃
Lead Temperature（Soldering，10sec.)	-	260	℃

Over operating temperature range (unless otherwise noted)(1)

Note:(1)Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute－maximum－rated conditions for extended periods may affect device reliability.

（2）All voltage values are with respect to network ground terminal

➢ Recommended Operating Conditions

PARAMETER	Min	Max	Unit
VIN Voltage(V_{IN})	4.5	17	V
Output current(I_{OUT})	0	4	A
TJ	-40	125	℃

Note : (1)All limits specified at room temperature (TA = 25°C) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

➢ ESD Ratings

PARAMETER	Description	Value	Unit
HBM	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
CDM	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	V

Note : (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

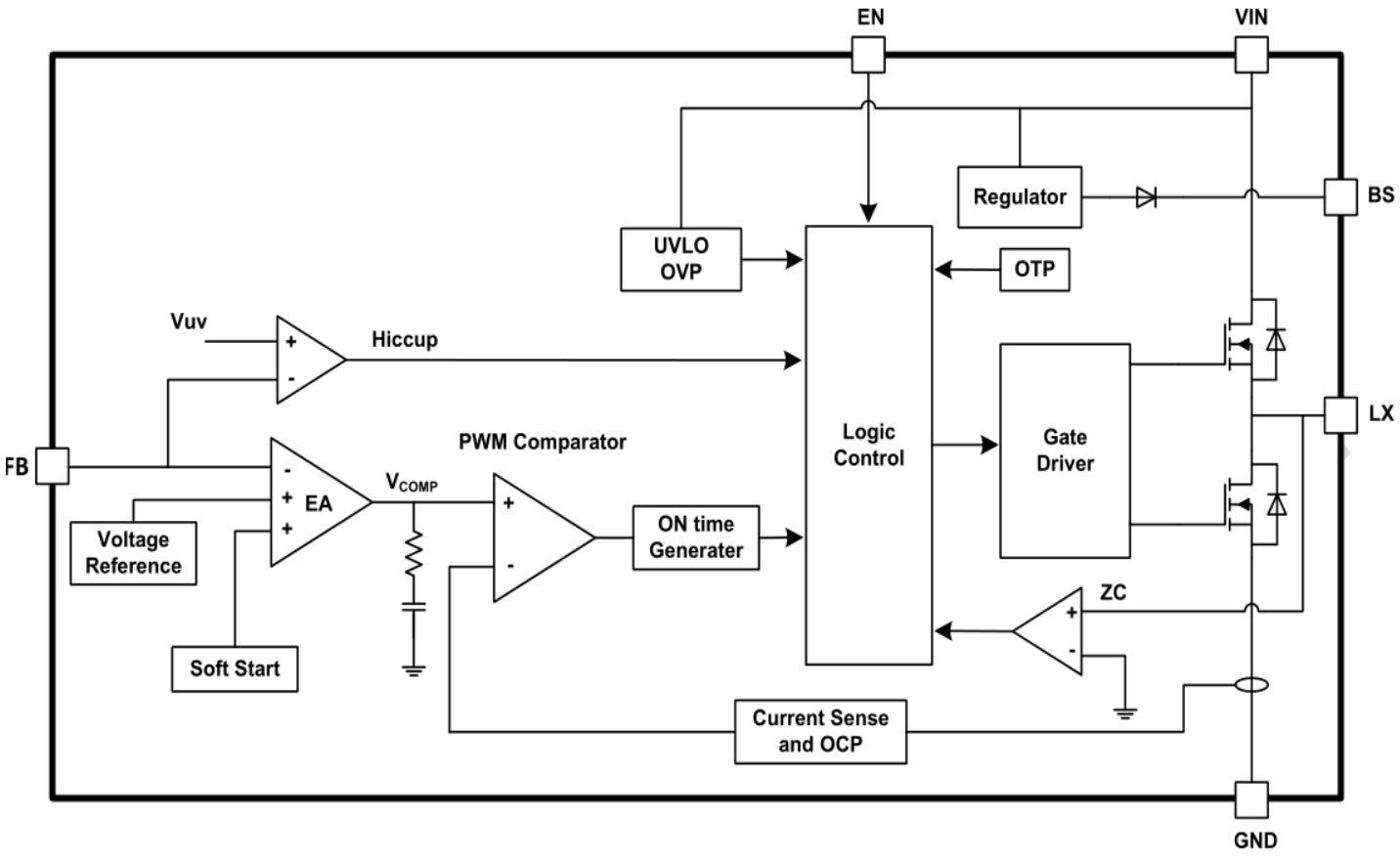
➢ Thermal Information

THERMAL METRIC	Description	TSOT23-6	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)(2)	54	℃/W

Note (1): The package thermal impedance is calculated in accordance to JESD 51-7.

Note (2): Thermal Resistances were simulated on a 4-layer, JEDEC board

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS(Typical at Vin=12V,TJ=25°C, unless otherwise noted.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input Voltage	V_{IN}		4.5		17	V
VIN Quiescent Current	I_Q	No-switching, V_{EN}=12V, V_{FB}=V_{REF}*105%, Iout=0A		200		uA
VIN OVP Rising Threshold	$V_{OVP(R)}$	V_{IN} Rsing		18		V
VIN OVP Hysteresis	$V_{OVP(HYS)}$			0.3		V
Shutdown Current	I_{SHDN}	V_{EN}=0V		3		uA
VIN UVLO Rising Threshold	$V_{UVLO(R)}$	V_{IN} Rsing		4.2		V
VIN UVLO Falling Threshold	$V_{UVLO(F)}$	V_{IN} Falling		3.8		V
VIN UVLO Hysteresis	$V_{UVLO(HYS)}$			0.4		V
FB Voltage	V_{FB}	T_J=25℃	0.594	0.6	0.606	V
FB Leakage Current	$I_{FB(LkG)}$	T_J=25℃	-100	0	100	nA
Switching Frequency	Fsw	V_{OUT}=1.2V, Operation CCM		500		KHZ
Mini on Pulse Width	$T_{ON(MIN)}$			50		ns
Mini off Pulse Width	$T_{OFF(MIN)}$			200		ns
High-Side Switch Current Limit	$I_{HS(OC)}$	V_{IN}= 12V, V_{FB}=90%		7		A
Low-Side Switch Current Limit	$I_{LS(OC)}$	V_{IN}= 12V, V_{FB}=90%		4.7		A
High-Side MOS ON-Resistance	$R_{DSON(HS)}$	Isw=100mA		35		mΩ
Low-Side MOS ON-Resistance	$R_{DSON(LS)}$	Isw=100mA		15		mΩ
EN Rising Threshold	$V_{EN(R)}$	4.5V≦VIN≦17V	1.2			V
EN Falling Threshold	$V_{EN(F)}$	4.5V≦VIN≦17V			0.4	V
EN Hysteresis	$V_{EN(HYS)}$			0.2		V
Soft Start	Tss	10%*Vout to 90%*Vout		1		ms
EN Dealy Time	T_{DLY}			400		us
Over-Temperature Protection	T_{SD}			160		℃
Over-Temperature Protection hysteresis	$\triangle T_{SD}$			30		℃

TYPICAL CHARACTERISTICS

Test Condition: TA = 25℃, VIN=12V, Vout=5V, unless otherwise noted.

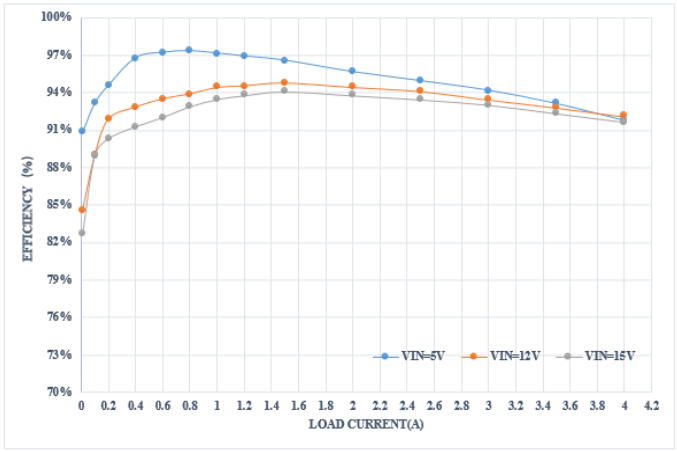


Figure1 5V Output Efficiency

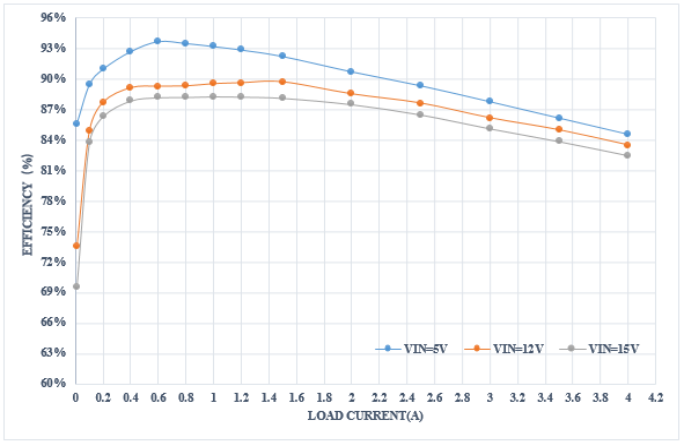


Figure2 1.2V Output Efficiency

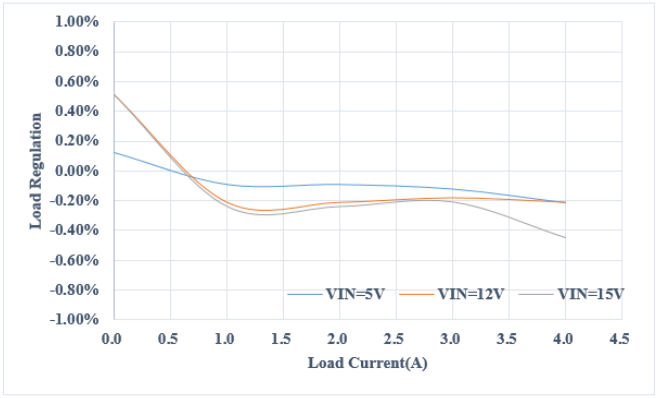


Figure3 5V Output Load Regulation

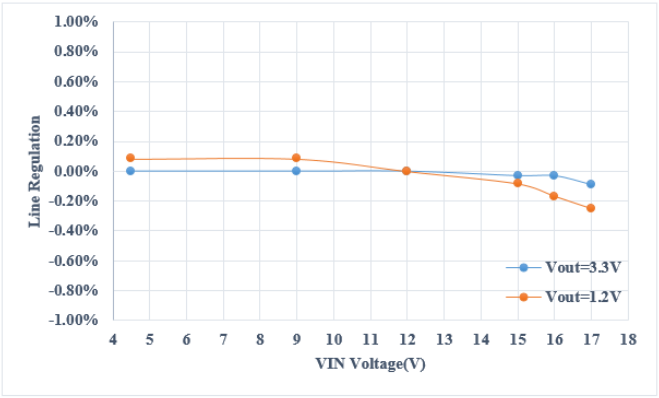
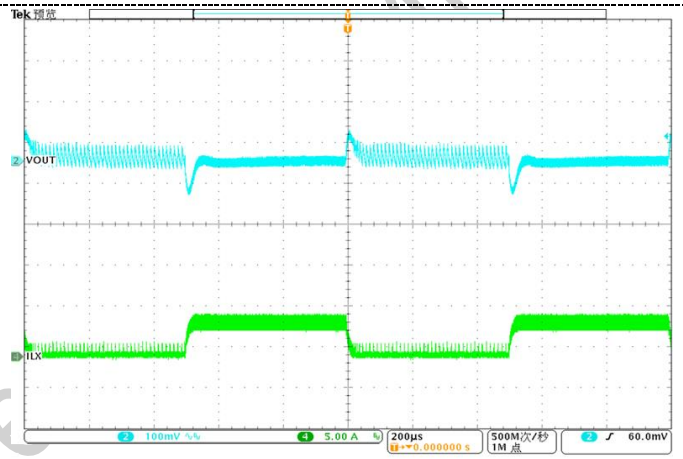
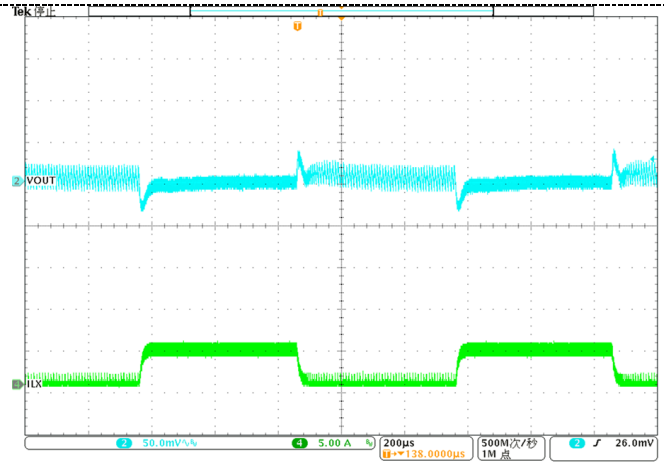


Figure4 Line Regulation



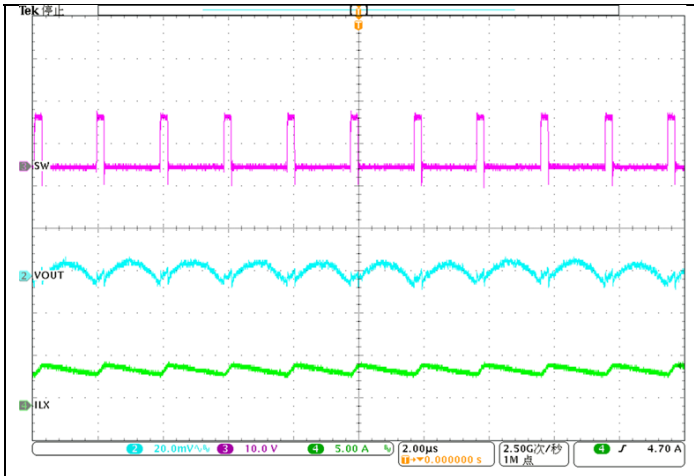
Load Step 1 to 4A, 1A/us Slew rate Vout=3.3V

Figure5 Load Transient



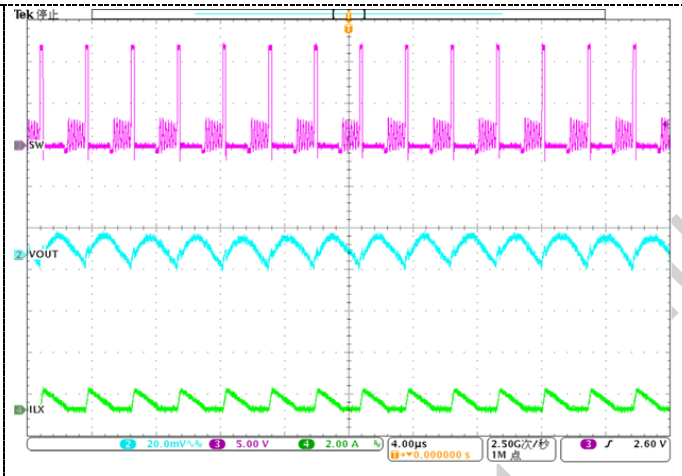
Load Step 1 to 4A, 1A/us Slew rate Vout=1.2V

Figure6 Load Transient



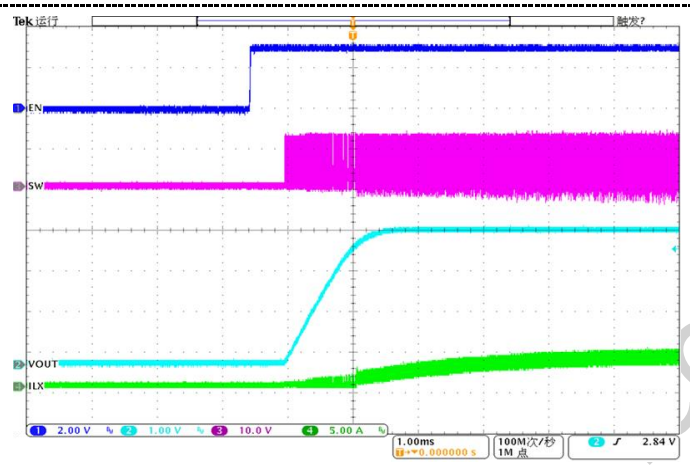
Iout=4A

Figure7 CCM Mode



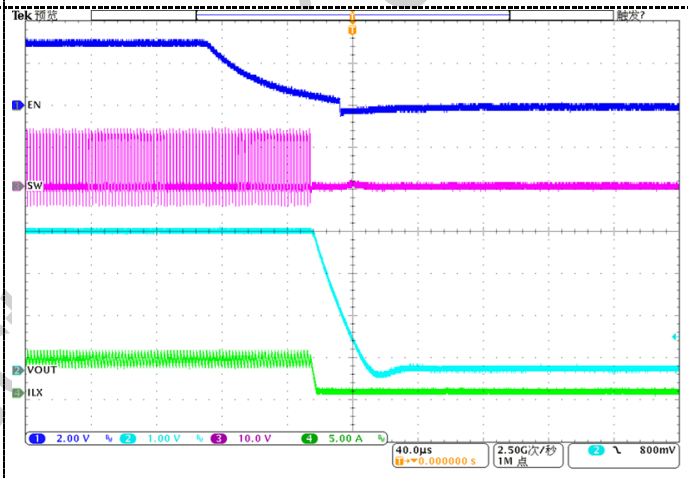
Iout=0.1A

Figure8 DCM Mode



Iout=4A

Figure9 EN StartUp with Load



Iout=4A

Figure10 EN ShutDown with Load

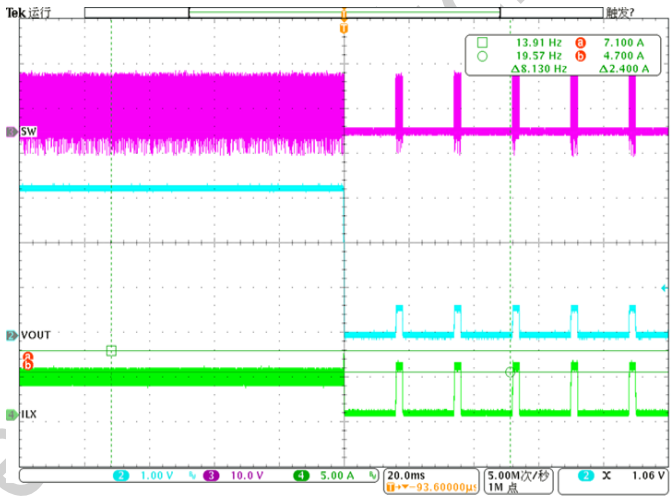


Figure11 Entry Short

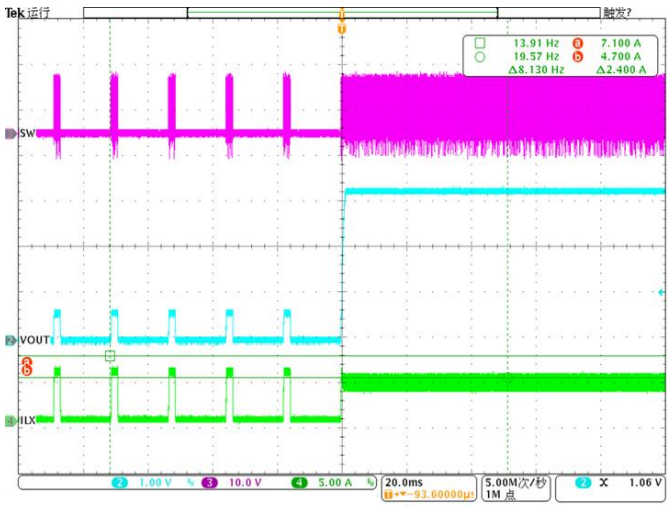


Figure12 Short Recovery

FUNCTIONS DESCRIPTION

The DP31214 Series is a COT mode step down DC/DC converter that provides excellent transient response with no extra external compensation components. This device contains an internal, low resistance, high voltage power MOSFET, and operates at a high 500KHz operating frequency to ensure a compact, high efficiency design with excellent DC performance.

- **Thermal Shutdown**

The internal thermal-shutdown circuitry forces the device to stop switching if the junction temperature exceeds 160 ° C typically. Once the junction temperature falls below the falling threshold, the device returns to normal operation automatically.

- **Soft Start**

The soft-start is implemented to prevent the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) ramping up from 0V to 0.768V. When it is lower than the internal reference (REF), SS overrides REF so the error amplifier uses SS as the reference. When SS is higher than REF, REF regains control. The SS time is internally max to 1200us.

- **Startup AND Shutdown**

The If both VIN and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries. Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault trigge ring. The comp voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

- **UNDER-VOLTAGE LOCKOUT (UVLO)**

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. When the voltage is higher than UVLO threshold voltage, the device is enabled again.

- **INPUT Over Voltage Protection(OVP)**

The DP31214S/FS Integrates input over voltage protection. The OVP circuitry detects over voltage condition by monitoring the input voltage. When input voltage rises above the OVP threshold , the OVP comparator turns high and both HS-FET and LS-FET are turned off. Once VIN drops below OVP falling threshold, the IC starts switching again. This function can ensure the reliability when the input voltage is unstable with over voltage spike.

- **Valley Over-Current Limit**

DP31214S/FS has a valley over-current limit control (OCL). The inductor current is monitored during the LS-FET on state. When the sensed inductor current reaches the valley current limit ($I_{LS(OC)}$), the LS limit comparator turns over, and the DP31214S/FS enters OCL mode. The HS-FET waits until the valley current limit is removed before turning on again. If the output load current exceeds the available inductor current (clamped by OCL), the output capacitor needs to supply the extra current so that the output voltage will begin to drop. If it drops below the output under-voltage protection threshold (V_{UVP}), the IC will stop switching into UV hiccup mode to avoid excessive heat.

- **Negative Over-Current Limit (DP31214FS Only)**

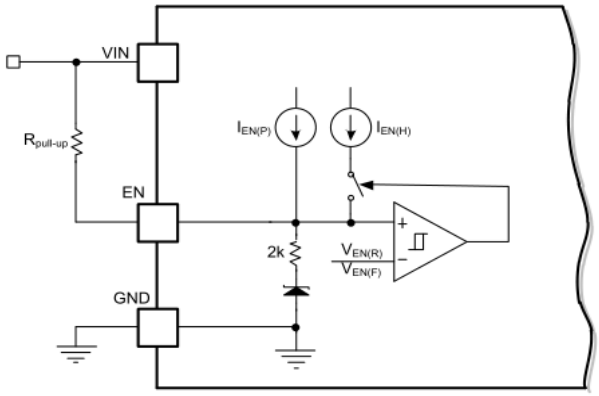
DP31214FS is the part which is FPWM part and allows negative current operation. In case of FPWM operation, high negative current may be generated as an external power source is tied to output terminal unexpectedly. As the risk described above, the internal circuit monitors negative current in each on-time interval of low- side MOSFET and compares it with negative over-current limit threshold (INoc). Once the negative current exceeds the NOC threshold, the low-side MOSFET is turned off immediately, and then the high-side MOSFET will be turned on to discharge the energy of output inductor. This behavior can keep the valley of negative current at NOC threshold to protect low-side MOSFET. Note that the NOC limit is not in effect during minimum off-time period.

- **Enable Control**

When the EN pin voltage rises above the rising threshold voltage ($V_{EN(R)}$) while the VIN voltage is higher than VIN under-voltage lock-out threshold, the device turs on. If the EN pin voltage is pulled below the falling threshold voltage, the regulator stops switching and enters the shutdown mode, that is, the regulator is disabled, and switching is inhibited even if the VIN voltage is above vin under-voltage Lock-out threshold. During shutdown mode. The supply current can be reduced to $I_{SHDN(VIN)}$(typical2.5μA).

The EN pin has an internal pull up source current which allows users to float the EN pin to enable the device, If an application requires control of the EN pin, external control logic interface like open drain or open-collector output logic can be connected to the EN pin. EN pin is clamped internally using a 5V series zener diode (typical break-down voltage is 6.9V). Connecting the EN input through a pull-up resistor
(>100kΩ) to VIN limits the EN input current to prevent damage to the zener diode.

When connecting the EN pin externally to a voltage higher than 6V,such as VIN voltage, a pull-up resistor (no less than100k is recommended)should be added in series to limit the input current of the EN pin and prevent damage to the zener diode, as shown in follow



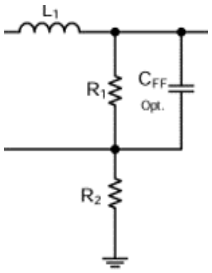
APPLICATION INFORMATION

The output stage of synchronous buck converter is mainly composed of inductor and capacitors. By switching the internally integrated power MOSFET, the energy is stored and transferred to the load, and the second-order LC filter is formed to smooth the switching node voltage so that the stable output DC voltage is obtained.

- **Setting Output Voltage**

The output voltage is set by FB voltage, which is divided by resistor (R1 & R2) from output node to Ground. That resistor with 1% or higher accuracy is preferred. The output voltage value is set by equation as below.

$V_{OUT}=V_{FB} \times ((R1+R2)/R2)$



Vref is the internal reference voltage of DP31214S/FS, 0.6V.

Table1 Recommend Component Selection Table

VOUT (V)	R1 (kΩ)	R2 (kΩ)	BS (uF)	L1 (uH)	CIN (uF)	COUT (uF)	CFF(pF) Opt.
1.0	6.8	10	0.1	1R0~4R7	22	68	OPT.
1.05	7.5	10	0.1	1R0~4R7	22	68	OPT.
1.2	10	10	0.1	1R0~4R7	22	68	OPT.
1.5	15	10	0.1	1R0~4R7	22	68	OPT.
1.8	20	10	0.1	2R2~4R7	22	68	OPT.
3.3	45	10	0.1	2R2~4R7	22	68	OPT.
5.0	73.2	10	0.1	4R7	22	68	OPT.

- **Inductor selection**

An inductor is required to supply constant current to the load while being driven by the switched input voltage. The common value of the inductance is between 1uH to 22uH. A larger value inductor will result in less current ripple and lower output voltage ripple. However, the larger value inductor will have larger physical size, higher DC resistance, and/or lower saturation current. A good rule to calculate the inductance is to allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum load current. At the same time, it is needed to make sure that the peak inductor current is below the inductor saturation current.

The inductance value can be calculated by:

$$L=\frac{V_{OUT}}{f_s \times \Delta I_L}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

Where VOUT is the output voltage, VIN is the input voltage, fs is the switching frequency, and ΔL is the peak-to-peak inductor ripple current.

The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

The choice of which style inductor to use mainly depends on the price vs. size requirements and any EMI constraints.

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency

- **Input capacitors selection**

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the converter. It is recommend to use low ESR capacitors to optimize the performance. Ceramic capacitor is preferred, but tantalum or low-ESR electrolytic capacitors may also meet the requirements. It is better to choose X5R or

X7R dielectrics when using ceramic capacitors.

Since the input capacitor (CIN) absorbs the input switching current, a good ripple current rating is required for the capacitor. The RMS current in the input capacitor can be estimated by:

$$I_{CIN}=I_{load}\times\sqrt{\frac{V_{OUT}}{V_{IN}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)}$$

The worst-case condition occurs at VIN = 2×VOUT, where:

$$I_{CIN}=\frac{I_{load}}{2}$$

For simplification, choose the input capacitor whose RMS current rating is greater than half of the maximum load current. When electrolytic or tantalum capacitors are used, a small, high quality ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible. When ceramic capacitors are used, make sure that they have enough capacitance to maintain voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN}=\frac{I_{load}}{f_s\times C_{IN}}\times\frac{V_{OUT}}{V_{IN}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

CIN is the input capacitance.

- **Output capacitors selection**

The output capacitor (COUT) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT}=\frac{V_{OUT}}{f_s\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times\left(R_{ESR}+\frac{1}{8\times f_s\times C_{OUT}}\right)$$

Where L is the inductor value, RESR is the equivalent series resistance (ESR) value of the output capacitor and COUT is the output capacitance value. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly determined by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT}=\frac{V_{OUT}}{8\times f_s^{2}\times L\times C_{OUT}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT}=\frac{V_{OUT}}{f_s\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The DP31214S/FS can be optimized for a wide range of capacitance and ESR values.

- **Feed-Forward Capacitor Selector(CFF)**

DP31214S/FS has internal loop compensation, so adding CFF is optional. Specifically, consider whether to add feed-forward capacitors according to the situation.

The use of a feed-forward capacitor (CFF) in the feedback network is to improve the transient response or higher phase margin. To reduce transient ripple, the feed-forward capacitor value can be increased to push the cross frequency to higher region. Although this can improve transient response, it also decreases phase margin and cause more ringing. In the other hand, if more phase margin is desired, the feed-forward capacitor value can be decreased to push the cross frequency to lower region.

the value of feed-forward capacitor (CFF) can be calculated with the following equation:

$$C_{ff\_op}=\frac{1}{2\pi\times f_{\_nocff}}\times\sqrt{\frac{1}{R1}\times\left(\frac{1}{R1}+\frac{1}{R2}\right)}$$

Wl _ ,uency. the crossing frequency is generally taken as 1/10 to 1/5 of the switching frequency, R1 and R2 are feedback resistors.

- **Bootstrap Capacitor Selection**

Bootstrap Capacitor Selection A 0.1-μF ceramic capacitor must be connected between the VBST to SW pin for proper operation. recommends to use a ceramic capacitor.

- **PCB Layout**

PCB layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion efficiency, thermal performance, and minimized EMI.

1. The feedback network, resistor R1 and R2, should be kept close to FB pin. Vout sense path should stay away from noisy nodes, such as SW & BS signals and preferably through a layer on the other side of shielding layer.

2. The input bypass capacitor Cin must be placed as close as possible to the VIN pin and ground.

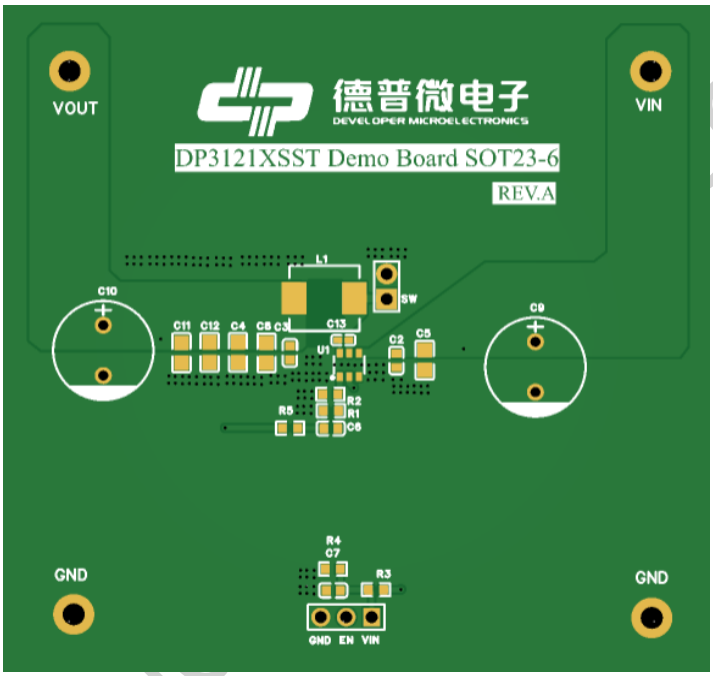
Grounding for both the input and output capacitors should consist of localized top side planes that connect to the GND pin and PAD. It is a good practice to place a ceramic cap near the VIN pin to reduce the high frequency injection current.

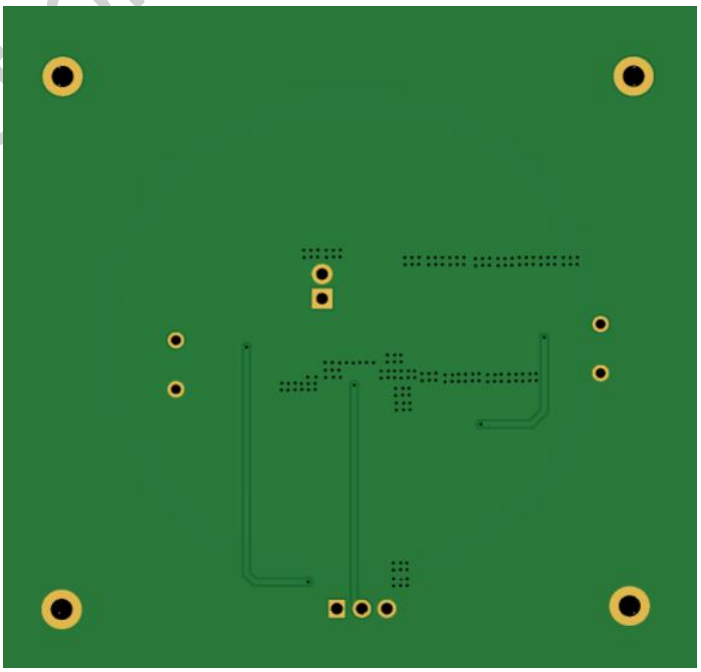
3. The inductor L should be placed close to the SW pin to reduce magnetic and electrostatic noise.

4. The output capacitor, COUT should be placed close to the junction of L. The L, and COUT trace should be as short as possible to reduce conducted and radiated noise and increase overall efficiency.

5. The ground connection for Cin and COUT should be as small as possible and connect to system ground plane at only one spot (preferably at the COUT ground point) to minimize injecting noise into system ground plane.

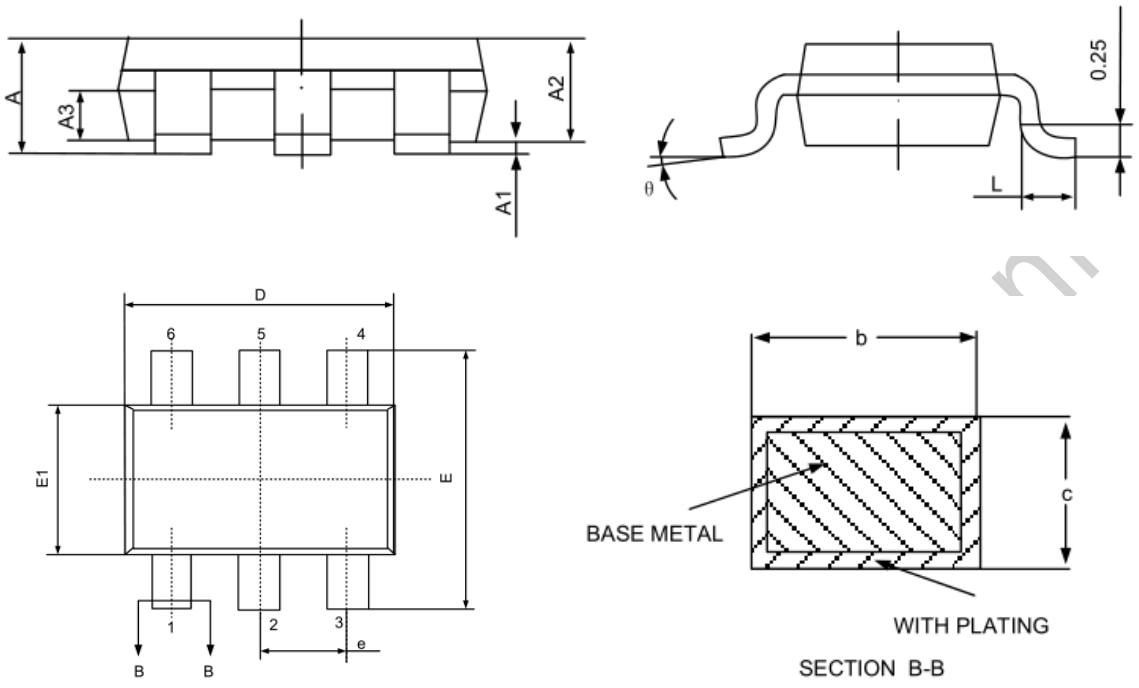
6. Large GND Copper Pour near IC is recommended to minimize the heat of IC.





PACKAGE DIMENSION

TSOT23-6



Symbol	Dimensions in Millimeters	
	Min	Max
A	-	0.950
A1	0.000	0.150
A2	0.750	0.850
A3	0.350	0.450
b	0.300	0.500
c	0.077	0.200
D	2.700	3.100
E1	1.500	1.700
E	2.600	3.000
e	0.950(BSC)	
L	0.300	0.500
θ	0°	8°

REVISION HISTORY

Editions	Revised Date	Redaction person	Revision content
A.0	2023/5/20	PXB	First release

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