300mA Ultra-Low Quiescent Current CMOS Low Dropout Regulator

FEATURES

- Low Dropout Voltage：120mV@100mA
- Low Quiescent Current：0.8μA(typ.)
- High Ripple Rejection：50dB@1kHz
- Excellent Line and Load Transient Response
- Operating Voltage Range：1.8V～6.0V
- Output Voltage Range：1.0V ~ 5.0V
- High Accuracy：±2%（Typ.)
- Low Output Noise:
  27*Voutμ VRMS(10Hz~100kHz)
- 300mA Output Current
- Built-in Current Limiter ,Short-Circuit Protection
- With Output Automatic Discharge
- Available in Green XTDFN-1×1-4L and
SOT23-5 Packages

DESCRIPTIONS

The DP31303 series are a group of positive voltage regulators manufactured by CMOS technologies with ultra low power consumption and low dropout voltage, which provide large output currents even when the difference of the input-output voltage is small.

The DP31303 series can deliver 300mA output current and allow an input voltage as high as 6V. The series are very suitable for the battery-powered equipments, such as RF applications and other systems requiring a quiet voltage source.

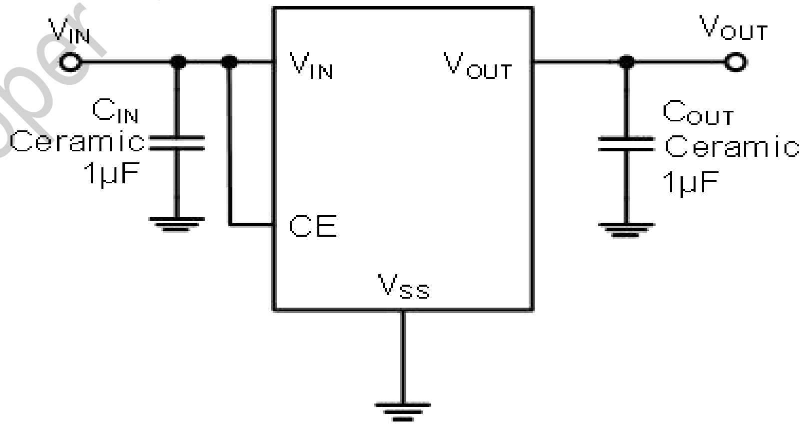
APPLICATIONS

- Portable Electronic Devices
- Smoke Detectors
- IP Cameras
- Wireless LAN Devices
- Battery-Powered Equipment
- Smartphones and Tablets
- Digital Cameras and Audio Devices

ORDERING INFORMATION

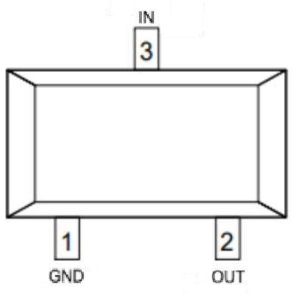
Part Number	Description
SOT23-5	Pb free in T&R, 3000 Pcs/Reel
SOT23-3	Pb free in T&R, 3000 Pcs/Reel
XTDFN-1×1-4L	Pb free in T&R, 10000 Pcs/Reel

TYPICAL APPLICATION CIRCUIT

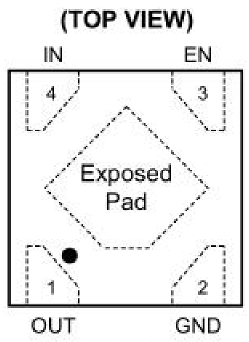


PRODUCT DESCRIPTION

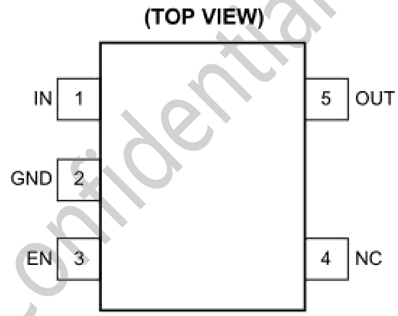
➢ Pin Arrangement



SOT-23-3



XTDFN-1×1-4L

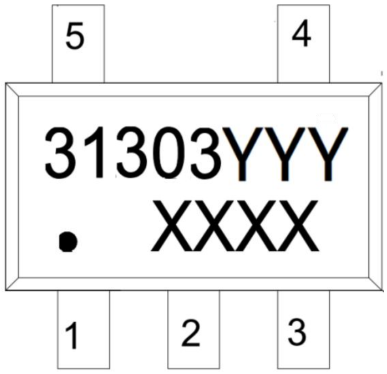


SOT-23-5

➢ Pin Configuration

SOT23-5	SOT23-3	XTDFN-1×1-4L	Pin Name	Description
1	3	4	IN	Input Supply Voltage Pin. It is recommended to use a 1μF or larger ceramic capacitor from IN pin to ground to get good power supply decoupling. This ceramic capacitor should be placed as close as possible to IN pin.
2	1	2	GND	Ground.
3	-	3	EN	Chip Enable Pin. Drive EN above 1.5V to turn on the part. Drive EN below 0.3V to turn it off. Do not leave EN floating.
4	-	-	NC	No Connection.
5	2	1	OUT	Regulator Output Pin. It is recommended to use a ceramic capacitor with effective capacitance in the range of 1μF to 10μF to ensure stability. This ceramic capacitor should be placed as close as possible to OUT pin.
-	-	Exposed Pad	GND	Exposed Pad. Connect it to a large ground plane to maximize thermal performance.

➢ Marking Information



DP31303 for product name:

YYY refers to the following table description, represents different packaging and special output voltage

XXXX The first X represents the last year,2020 is 0;The second X represents the month,inA-L 12 letters;The third and fourth X on behalf of the date,01-31said;

Marking	Model	VOUT Voltage	PACKAGE
310	DP31303-10ATD	1.0V	XTDFN-1×1-4L
105	DP31303-105ATD	1.05V	XTDFN-1×1-4L
311	DP31303-11ATD	1.1V	XTDFN-1×1-4L
312	DP31303-12ATD	1.2V	XTDFN-1×1-4L
315	DP31303-15ATD	1.5V	XTDFN-1×1-4L
318	DP31303-18ATD	1.8V	XTDFN-1×1-4L
325	DP31303-25ATD	2.5V	XTDFN-1×1-4L
328	DP31303-28ATD	2.8V	XTDFN-1×1-4L
330	DP31303-30ATD	3.0V	XTDFN-1×1-4L
333	DP31303-33ATD	3.3V	XTDFN-1×1-4L

336	DP31303-36ATD	3.6V	XTDFN-1×1-4L
342	DP31303-42ATD	4.2V	XTDFN-1×1-4L
31303-10	DP31303-10AST	1.0V	SOT23-5
31303105	DP31303-105AST	1.05V	SOT23-5
31303-11	DP31303-11AST	1.1V	SOT23-5
31303-12	DP31303-12AST	1.2V	SOT23-5
31303-15	DP31303-15AST	1.5V	SOT23-5
31303-18	DP31303-18AST	1.8V	SOT23-5
31303-25	DP31303-25AST	2.5V	SOT23-5
31303-28	DP31303-28AST	2.8V	SOT23-5
31303-30	DP31303-30AST	3.0V	SOT23-5
31303-33	DP31303-33AST	3.3V	SOT23-5
31303-36	DP31303-36AST	3.6V	SOT23-5
31303-42	DP31303-42AST	4.2V	SOT23-5
03-10	DP31303-10BST	1.0V	SOT23-3
03105	DP31303-105BST	1.05V	SOT23-3
03-11	DP31303-11BST	1.1V	SOT23-3
03-12	DP31303-12BST	1.2V	SOT23-3
03-15	DP31303-15BST	1.5V	SOT23-3
03-18	DP31303-18BST	1.8V	SOT23-3
03-25	DP31303-25BST	2.5V	SOT23-3

03-28	DP31303-28BST	2.8V	SOT23-3
03-30	DP31303-30BST	3.0V	SOT23-3
03-33	DP31303-33BST	3.3V	SOT23-3
03-36	DP31303-36BST	3.6V	SOT23-3
03-42	DP31303-42BST	4.2V	SOT23-3

Absolute Maximum Ratings

Over operating temperature range (unless otherwise noted)(1)

PARAMETER	Min	Max	Unit
VIN Voltage(1)	-0.3	7	V
EN Voltage	-0.3	7	V
VOUT Voltage(2)	-0.3	VIN+0.3	V
Output Current	-	300	mA
SOT-23 Power Dissipation	-	400	mW
Operating free air temperature range	-40	85	℃
Operating junction temperature,TJ	-40	150	℃
Storage temperature, Tstg	-65	150	℃
Lead Temperature（Soldering，10sec.)	-	260	℃

Note:(1)Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute – maximum – rated conditions for extended periods may affect device reliability.

（2）All voltage values are with respect to network ground terminal

Recommended Operating Conditions

PARAMETER	Min	Max	Unit
VIN Voltage(V_{IN})	1.8	6	V
VOUT Voltage(V_{OUT})	1	5	V
Output current(I_{OUT})	-	300	mA
TJ	-40	125	℃

Note : (1)All limits specified at room temperature (TA = 25°C) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

➢ ESD Ratings

PARAMETER	Description	Value	Unit
HBM	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
CDM	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±200	V

Note : (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

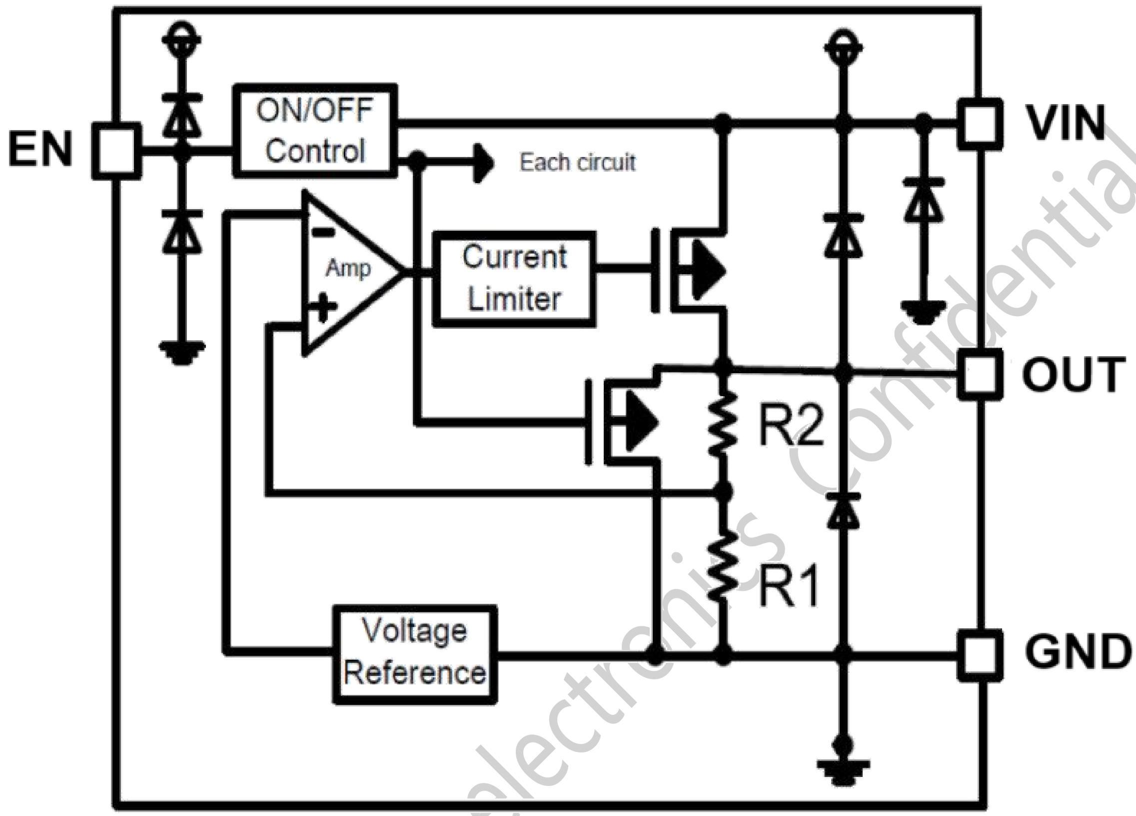
➢ Thermal Information

THERMAL METRIC	Description	SOT23-5	SOT23-3	XTDFN-1×1-4L	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)(2)	191.6	267.3	166.1	℃/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	141.4	103.5	103.6	℃/W
$R_{\theta JB}$	Junction-to-board(Bottom) thermal	44.5	98	110.6	℃/W
ψ_{JT}	Junction-to-top characterization parameter	34.5	9.2	3.0	℃/W
ψ_{JB}	Junction-to-board characterization	43.9	97.4	103.3	℃/W

Note (1): The package thermal impedance is calculated in accordance to JESD 51-7.

Note (2): Thermal Resistances were simulated on a 4-layer, JEDEC board

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

V_{IN}=V_{OUT}+1V, C_{IN}=C_{OUT}=1μF，T_A=25℃,unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input Voltage	V_{IN}	-	1.8	-	6	V
Output Voltage	V_{OUT}	I_{OUT}=1mA	VOUT* 0.99	-	VOUT* 1.01	V
Supply Current	I_Q	I_{OUT}=0mA		0.8	1.5	uA
Standby Current	I_{SHDN}	V_{EN}=0V		0.1	1	uA
Output Current	I_{OUT}	-		300		mA
Dropout Voltage	V_{DROP}	Iout=60mA Vout=2.8V		70		mV
		Iout=100mA Vout=2.8V		120		mV
		Iout=200mA Vout=2.8V		200		mV
Load Regulation	ΔV_{OUT}	V_{IN}= V_{OUT} +0.5V, 1mA≤I_{OUT}≤300mA		10		mV
Line Regulation	$\frac{\Delta V_{OUT}}{V_{OUT} \times \Delta V_{IN}}$	I_{OUT} =100mA V_{OUT} +1V≤V_{IN}≤6V		0.05	0.3	%/V
Output Voltage Temperature Characteristics	$\frac{\Delta V_{OUT}}{\Delta T \times V_{OUT}}$	I_{OUT} =10mA -40≤T≤+85℃		100		ppm
Short Current	Ishort	V_{OUT}=0V		100		mA
Power Supply Rejection Rate	PSRR	F=100HZ Iout=50mA		65		dB
		F=1KHZ Iout=50mA		50		
		F=10KHZ Iout=50mA		40		
EN Rising Threshold	$V_{EN(R)}$	1.8V≦VIN≦5.5V	1.5			V
EN Falling Threshold	$V_{EN(F)}$	1.8V≦VIN≦5.5V			0.3	V
Over-Temperature Protection	T_{SD}			160		℃
Over-Temperature Protection hysteresis	△TSD			20		℃
COUT Auto-Discharge Resistance	$R_{DISCHRG}$	V_{IN}=5V, V_{OUT}=3.0V, V_{CE}=V_{SS}		100		Ω

TYPICAL CHARACTERISTICS

TJ = +25℃, VIN = (VOUT(NOM) + 1V) (whichever is greater), VEN = VIN, CIN = COUT = 1μF, unless otherwise noted.

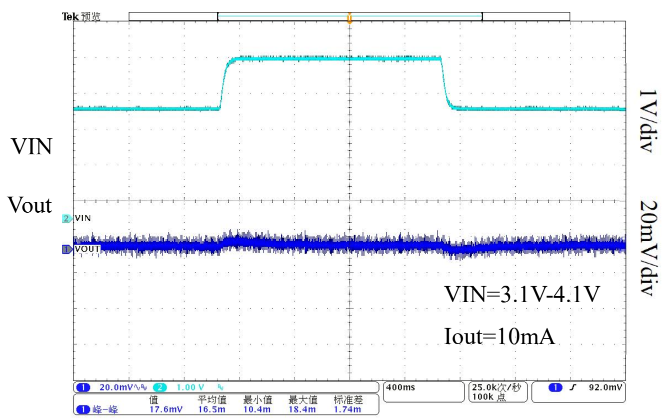


Figure1 Vout=2.8V Line Transient Response

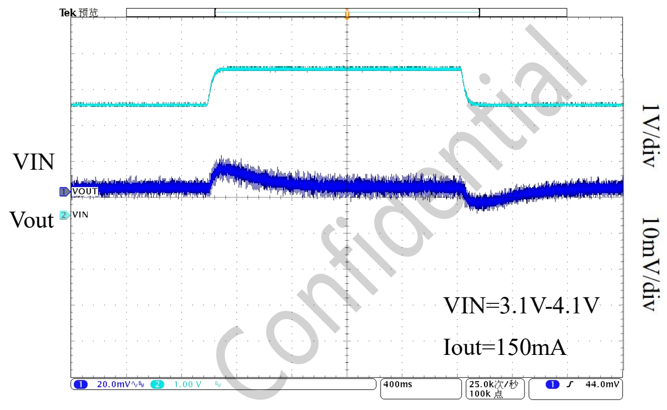


Figure2 VOUT=2.8V Line Transient Response

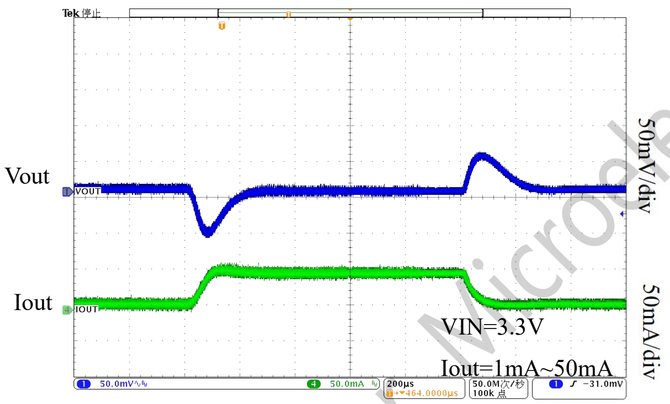


Figure3 Load Transient Response Vout=2.8V

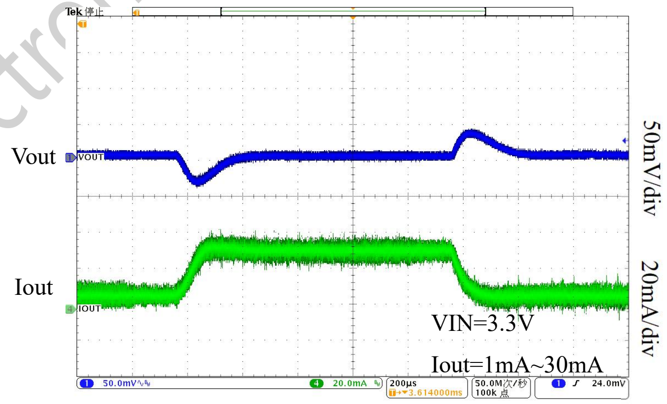


Figure4 Load Transient Response Vout=2.8V

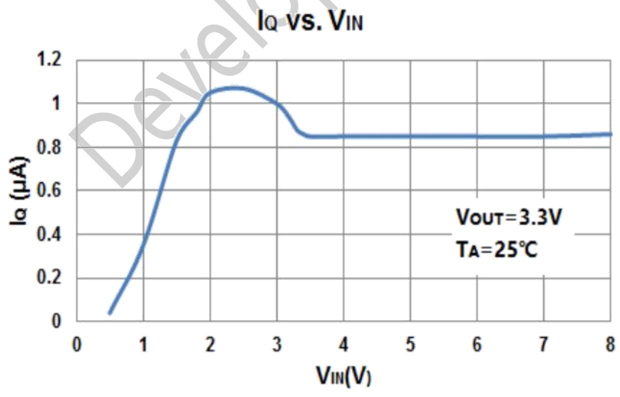


Figure5 Output Voltage vs. Temperature

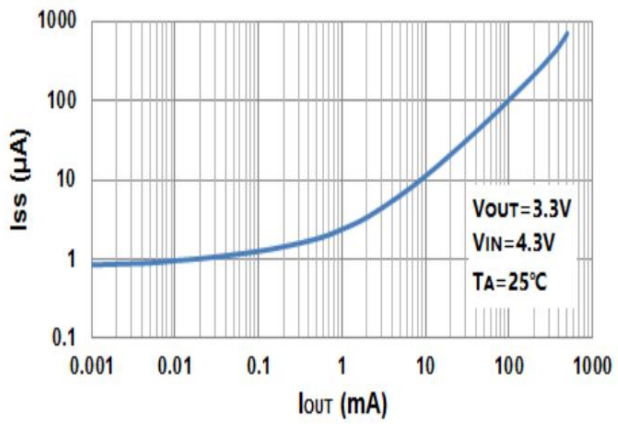


Figure6 Output Current vs Ground Current

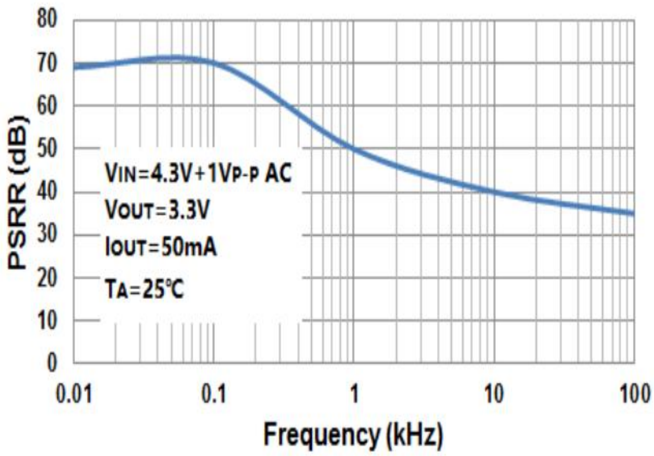


Figure7 Power Supply Rejection Ratio vs. Frequency

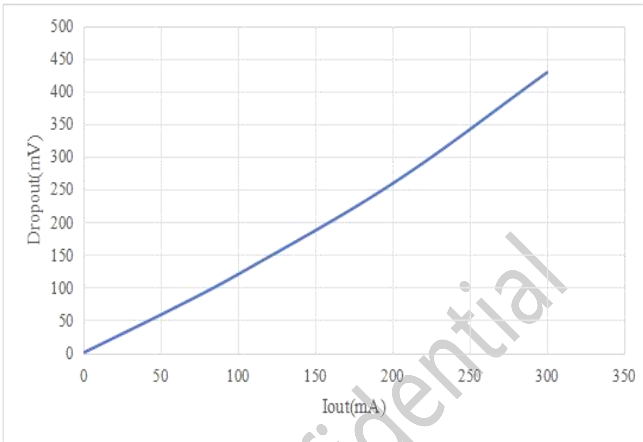


Figure8 Dropout vs Output Current

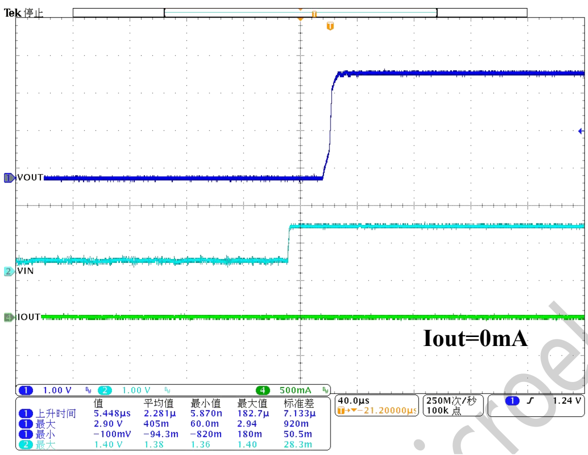


Figure9 EN Start Up with Load

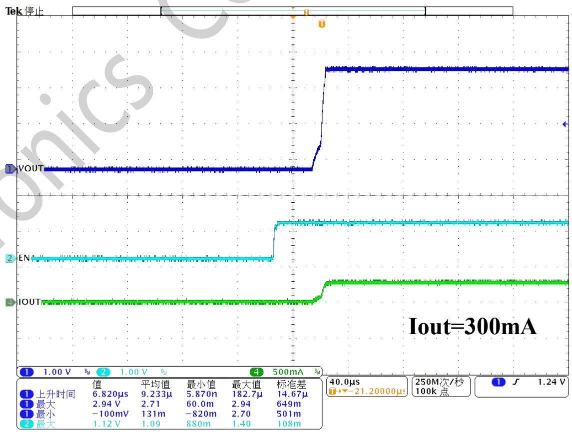
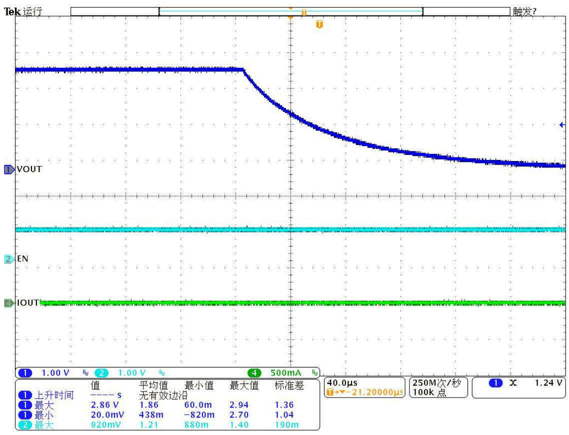
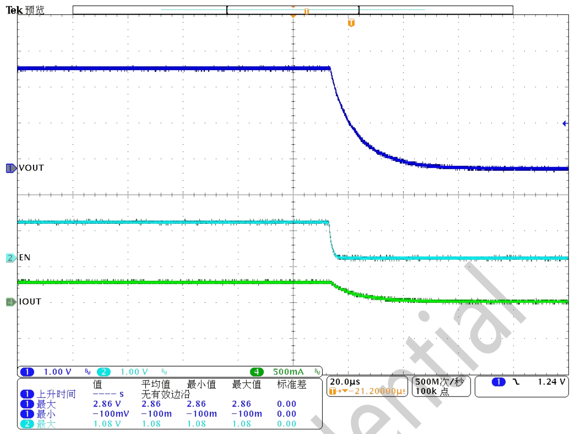


Figure10 EN Start Up with Load



Iout=0.01A

Figure11 EN Start Down with Load



Iout=0.3A

Figure12 EN Start Down with Load

APPLICATION INFORMATION

The DP31303 is an ultra-low quiescent current high performance LDO and provides 300mA output current. These features make the device a reliable solution to solve many challenging problems in the generation of clean and accurate power supply. The DP31303 also provides the protection functions for output overload, output short-circuit condition . The DP31303 provides an EN pin as an external chip enable control to enable/disable the device. When the regulator is in shutdown state, the shutdown current consumes as low as 0.05μA (TYP).

- **Input capacitors selection**

The input decoupling capacitor should be placed as close as possible to the IN pin to ensure the device stability. 1μF or larger X7R or X5R ceramic capacitor is selected to get good dynamic performance. When VIN is required to provide large current instantaneously, a large effective input capacitor is required. Multiple input capacitors can limit the input tracking inductance. Adding more input capacitors is available to restrict the ringing and to keep it below the device absolute maximum ratings.

- **Output capacitors selection**

The output capacitor should be placed as close as possible to the OUT pin. 1μF or larger X7R or X5R ceramic capacitor is selected to get good dynamic performance. The minimum effective capacitance of COUT that DP31303 can remain stable is 1μF. For ceramic capacitor, temperature, DC bias and package size will change the effective capacitance, so enough margin of COUT must be considered in design. Additionally, COUT with larger capacitance and lower ESR will help increase the high frequency PSRR and improve the load transient response.

- **Enable Operation**

The EN pin of the DP31303 is used to enable/disable its device and to deactivate/activate the output automatic discharge function. When the EN pin voltage is lower than 0.3V, the device is in shutdown state. There is no current flowing from IN to OUT pins. In this state, the automatic discharge transistor is active to discharge the output voltage through a 100Ω (TYP) resistor.
When the EN pin voltage is higher than 0.7V, the device is in active state. The output voltage is regulated to the expected value and the automatic discharge transistor is turned off.

- **Output Current Limit and Short-Circuit**

Protection

When overload events happen, the output current is internally limited to 500mA (TYP). When the OUT pin is shorted to ground, the short-circuit protection will limit the output current to 130mA (TYP).

- **PCB Layout**

PCB layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion efficiency, thermal performance, and minimized EMI.

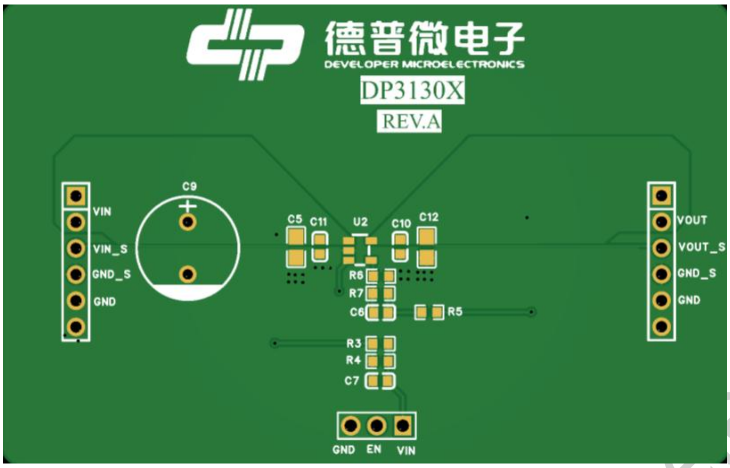
1. The input bypass capacitor C5 and C11 must be placed as close as possible to the VIN pin and ground. Grounding for both the input and output capacitors should consist of localized top side planes that connect to the GND pin and PAD. It is a good practice to place a ceramic cap near the VIN pin to reduce the high frequency injection current.

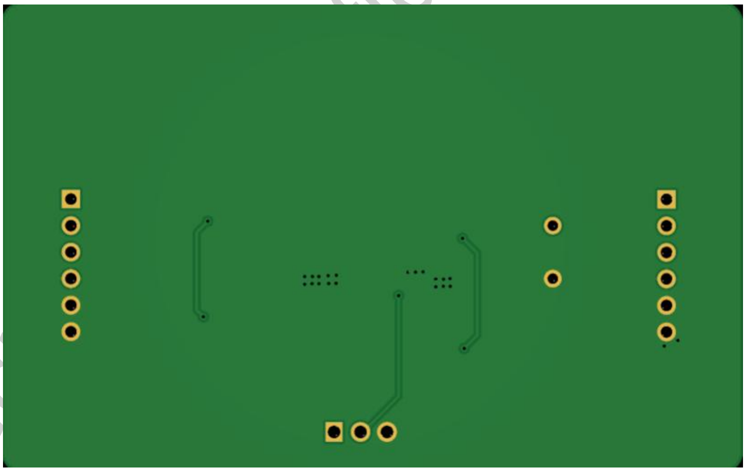
2. The output capacitor, COUT should be placed close to the junction of Vout Pin.

3. The ground connection for C5, C11 and C10, C12 should be as small as possible and connect to system ground plane at only one spot (preferably at the COUT ground point) to minimize injecting noise into system ground plane.

4. Large GND Copper Pour near IC is recommended to minimize the heat of IC.

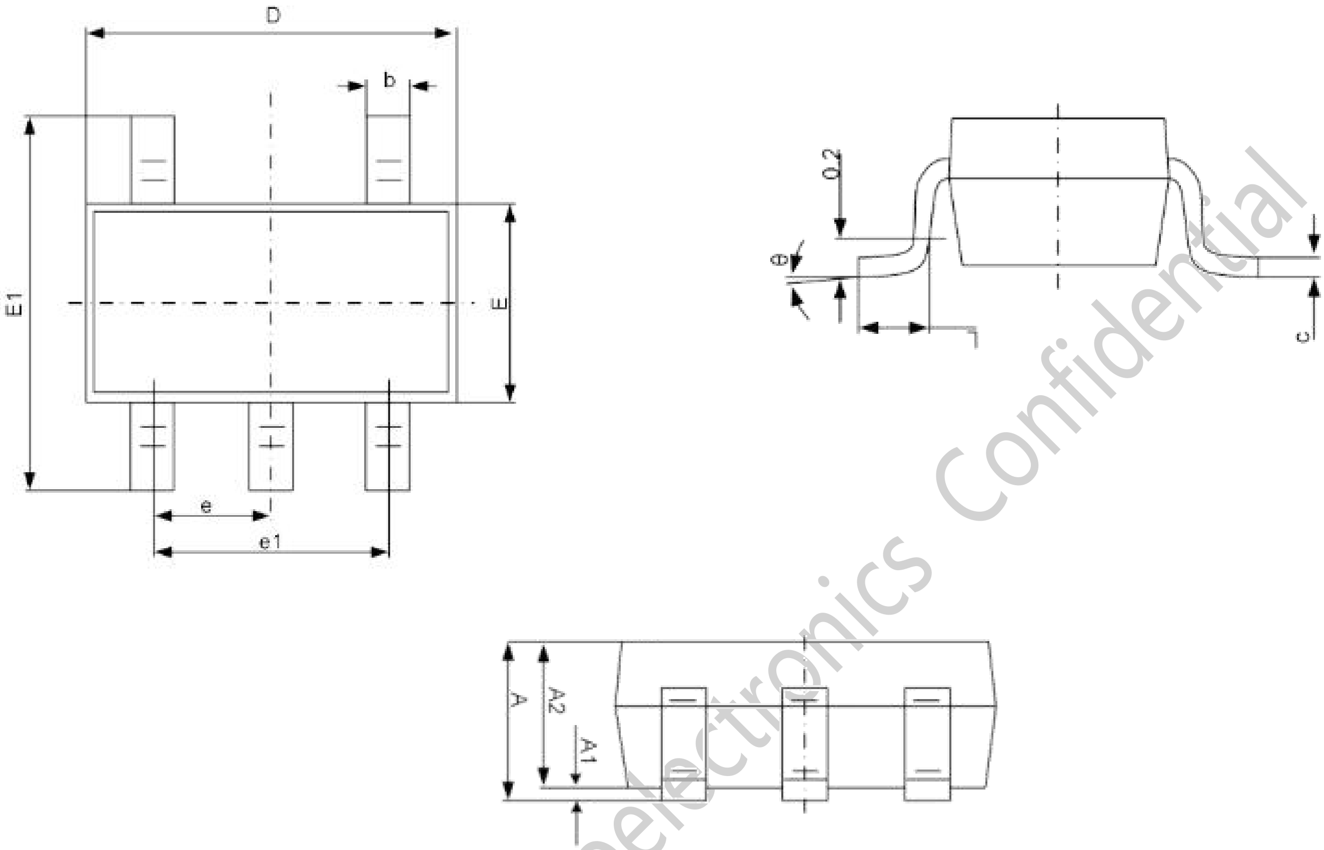
- **Layout Example:**





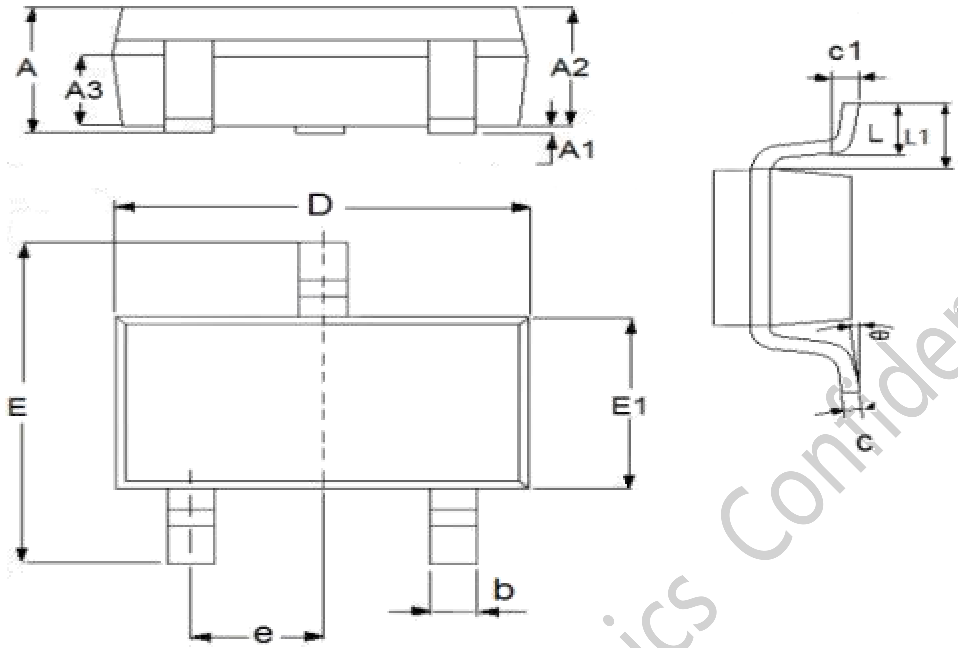
PACKAGE DIMENSION

SOT23-5



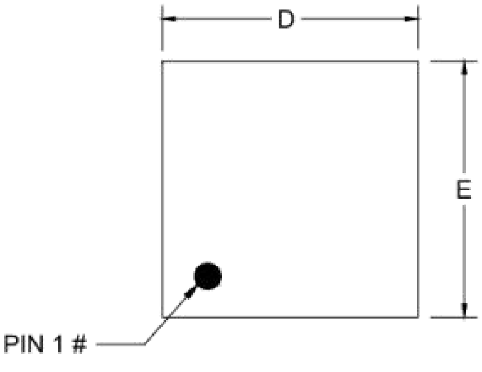
Symbol	Dimensions in Millimeters	
	Min	**Max**
A	-	1.350
A1	0.000	0.150
A2	1.000	1.200
b	0.300	0.500
c	0.100	0.220
D	2.820	3.020
E	1.500	1.700
E1	2.600	3.000
e	0.950(BSC)	
e1	1.800	2.000
L	0.300	0.600
θ	0°	8°

S0T23-3

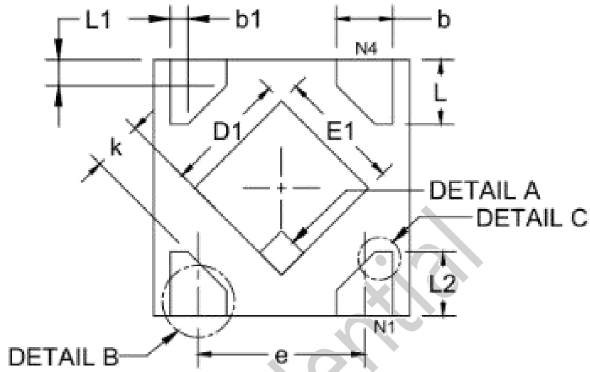


Symbol	Dimensions in Millimeters	
	Min	**Max**
A	1.050	1.450
A1	0.000	0.150
A2	0.900	1.300
A3	0.600	0.700
b	0.250	0.500
c	0.100	0.250
D	2.800	3.100
E	2.600	3.100
E1	1.500	1.800
e	0.950(TYP)	
L1	0.590(TYP)	
L	0.250	0.600
θ	0°	8°
c1	0.20(TYP)	

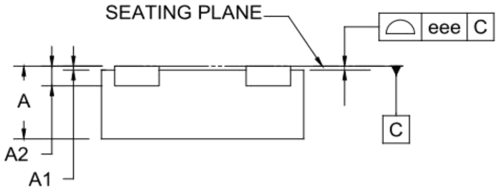
XTDFN_1*1-4L



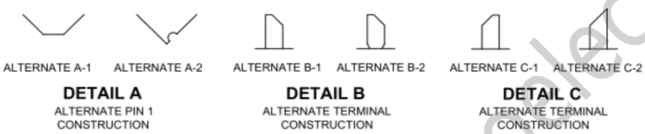
TOP VIEW

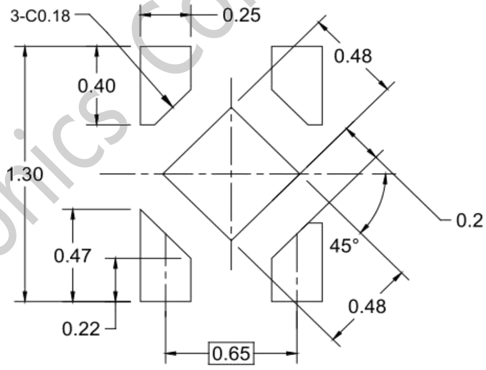


BOTTOM VIEW



SIDE VIEW





RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	Min	MOD	Max
A	0.340	0.370	0.400
A1	0.000	0.020	0.050
A2	0.100REF		
b	0.170	-	0.300
b1	0.068REF		
D	0.950	1.000	1.050
E	0.950	1.000	1.050
D1	0.430	0.480	0.530
E1	0.430	0.480	0.530
e	0.650(BSC)		
L	0.200	0.250	0.300
L1	0.093REF		
L2	0.200	-	0.370
k	0.150	-	-
eee	-	0.050	-

REVISION HISTORY

Editions	Revised Date	Redaction person	Revision content
REV1.0	2024/12/23	PXB	First release

OFFICIAL ANNOUNCEMENT

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Please note that the product is used within the conditions described in this document, paying particular attention to the absolute maximum rating, operating voltage range, and electrical characteristics. The Company shall not be liable for any damage caused by malfunctions, accidents, etc. caused by the use of the product outside the conditions stated in this document.

Division I has been committed to improving the quality and reliability of products, but all semiconductor products have a certain probability of failure, which may lead to some personal accidents, fire accidents, etc.When designing products, pay full attention to redundancy design and adopt safety indicators, so as to avoid accidents.

When using our chips to produce products, Division I shall not be liable for any patent dispute arising from the use of the chip in the product, the specification of the product, or the country of import, etc., in the event of a patent dispute over the products including the chip.