High Performance Primary Side Regulation CV/CC Power Switch

FEATURES

- Built-in 800V High Voltage Power BJT
- PSR Control, High Efficiency
- Multi-mode PSR Control
- Fast Dynamic Response
- Integrated Dynamic BJT Driving Circuit
- Optimized EMI Performance
- Audio Noise Free Operation
- CC and CV regulation ±5%
- Low Standby Power <30mW
- Cable Drop Compensation
- Build-in Protections:
  - Short Load Protection (FB SLP)
  - Over Voltage Protection (FB OVP)
  - Cycle-by-Cycle Current Limiting (OCP)
  - On-Chip Thermal Shutdown (OTP)
  - VDD OVP & UVP & Clamp
- Available with SOP7/SOP8 Package

GENERAL DESCRIPTION

DP2312HTFA is a high performance Primary Side Regulation (PSR) PWM power switch with high precision CV/CC control ideal for charger applications , especially for low power off-line charger.

DP2312HTFA can achieve audio noise free operation and fast dynamic response. The built-in Cable Drop Compensation (CDC) function can provide excellent CV performance.

DP2312HTFA integrates functions and protections of VDD Under Voltage Lockout (UVLO), VDD over Voltage Protection (VDD OVP), Cycle-by-cycle Current Limiting (OCP), Short Load Protection (SLP), On-Chip Thermal Shutdown (OTP), VDD Clamping, etc.

DP2312HTFA also integrates single failure protections, including FB pull-up resistor open protection, FB pull-down resistor open protection, FB pull-down resistor short protection, output rectifier diode or SR open protection, output rectifier diode or SR short protection, transformer windings short protection and R_{CS} open protection.

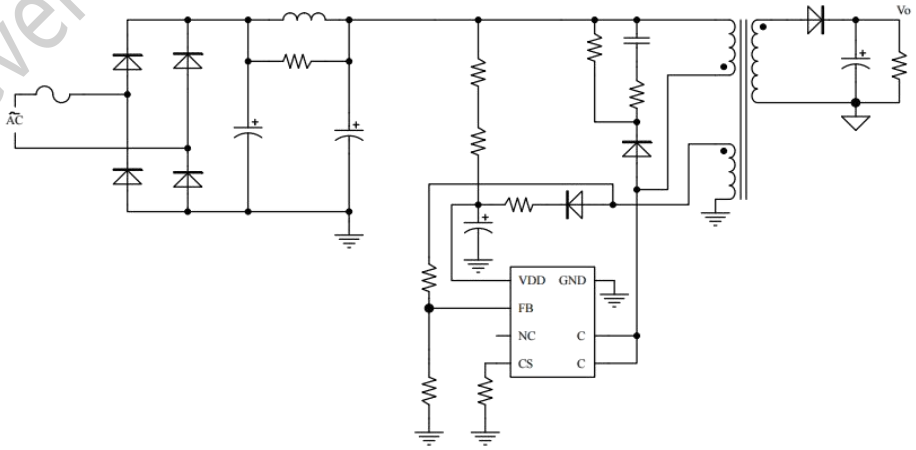
APPLICATIONS

- Battery Chargers for Cellular Phones
- AC/DC Power Adapter

PACKAGE

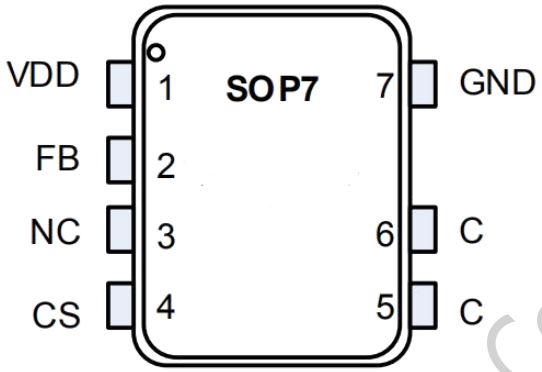
Name	Description	MSL
DP2312HTFA	SOP7, Halogen free, Reel, 4000pc/reel	3

TYPICAL APPLICATIONI CIRCUIT



PRODUCTS DESCRIPTION

➢ PIN CONFIGURATION



➢ PIN DISCRIPTION

PIN Number	PIN Name	I/O	PIN Description（SOP7）
1	VDD	P	IC Power supply pin
2	FB	I	System feedback pin which regulates both the output voltage in CV mode and output current in CC mode based on the flyback voltage of the auxiliary winding.
3	NC	-	No connect
4	CS	I	Current Sense Input Pin
5,6	C	P	Internal Power BJT collector pin
7	GND	P	IC Ground pin

➢ MARKING INFORMATION

DP2312HTFA for product name:

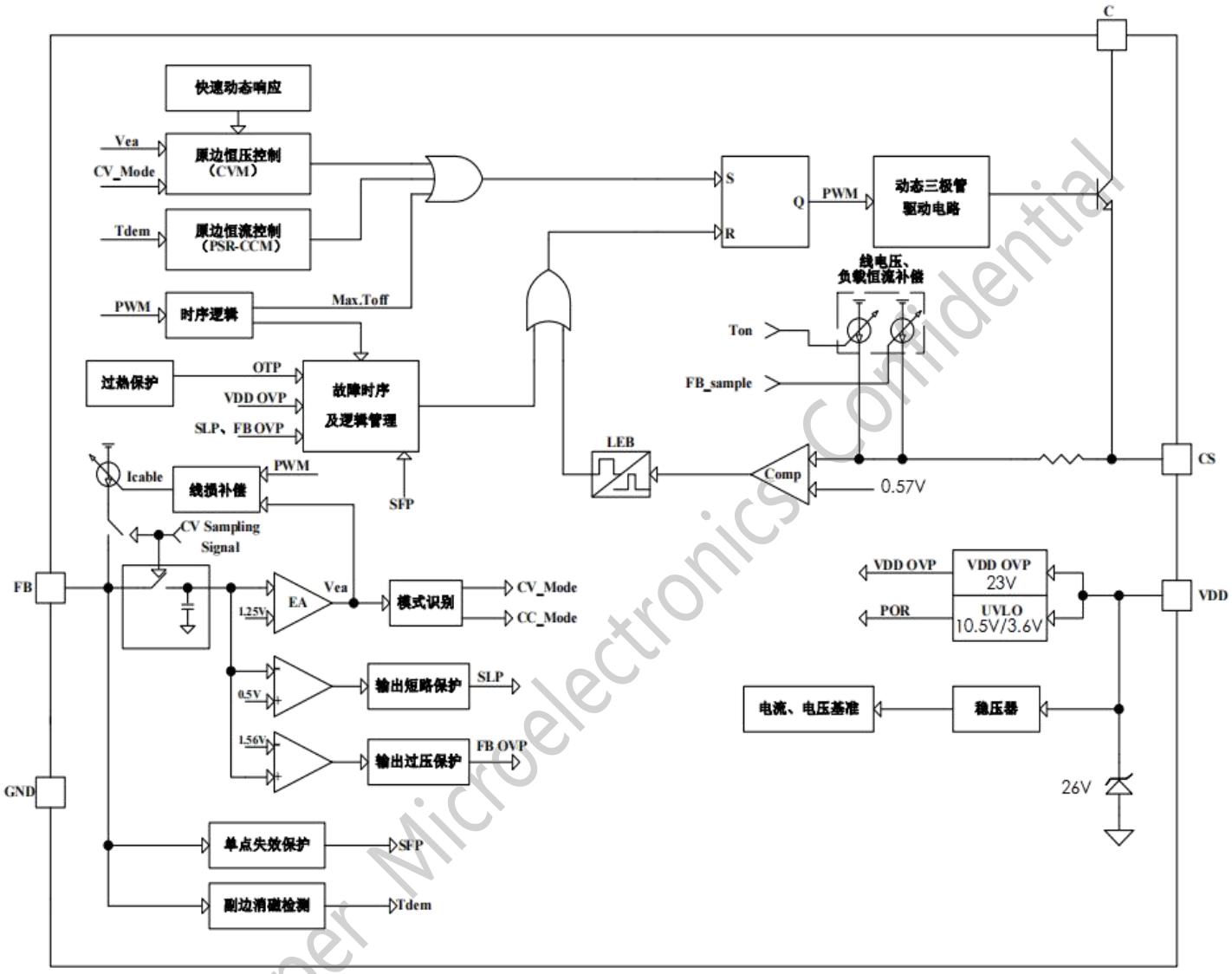
XXXXXX, the first X represents the last NO of year, 2014 is 4; The second X represents the month, in A-L 12 letters; The third and fourth X on behalf of the date, 01-31 said; The last X represents the wafer batch code.

➢ TYPICAL OUTPUT POWER TABLE

Part Number	230VAC ± 15%(2)	85-265VAC
	Adapter (3)	**Adapter** (3)
DP2313HFTA	6W	5W

Note 1. The Max. output power is limited by junction temperature.
Note 2. 230VAC or 100/115VAC with voltage doubler.
Note 3. Typical continuous power in a non-ventilated enclosed adapter with sufficient collector pattern as a heat sink at 50℃ ambient.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(Note 4)

Parameter	Value	Unit
C Pin Voltage Range	-0.3 to 800	V
VDD DC Supply Voltage	-0.3 to 28	V
VDD DC Clamp Current	7	mA
CS Voltage Range	-0.3 to 7	V
FB Voltage Range	-0.7 to 7	V
Package Thermal Resistance---Junction to Ambient (SOP7)	90	℃/W
Maximum Junction Temperature	165	℃
Storage Temperature Range	-65 to150	℃
Lead Temperature (Soldering, 10sec.)	260	℃
ESD Capability, HBM (Human Body Model)	3	KV

RECOMMENDED OPERATION CONDITIONS

Parameter	Value	Unit
Supply Voltage, VDD	5 to 20	V
Operating Ambient Temperature	-40 to 85	℃
Maximum Switching Frequency @ Full Loading	70	kHz
Minimum Switching Frequency @ Full Loading	35	kHz

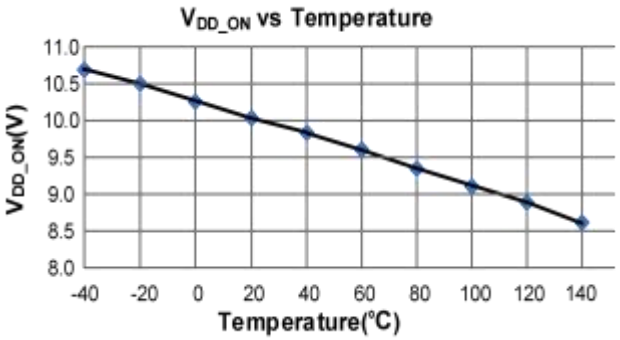
ELECTRICAL CHARACTERISTICS (TA= 25℃,VDD=16V, If not otherwise noted)

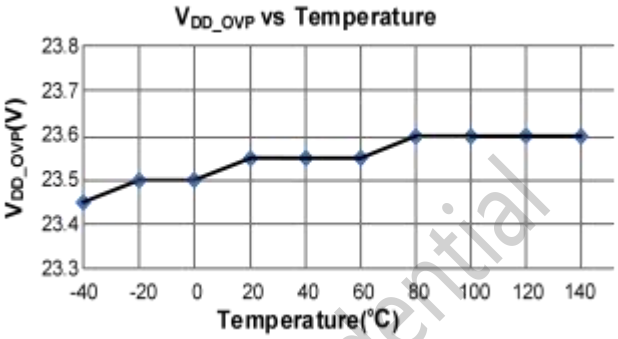
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
Supply Voltage Section (VDD Pin)						
IVDD_st	Start-up current into VDD pin	VDD< VDD_ON	0.1	1.1	3	uA
IVDD_op	Operation Current			0.8	1.5	mA
IVDD_standby	Standby Current		0.12	0.26	0.5	mA
VDD_ON	VDD Under Voltage Lockout Exit		9	10	12	V
VDD_OFF	VDD Under Voltage Lockout Enter		2.6	3.6	4.5	V
VDD_OVP	VDD OVP Threshold		21	23	25	V
VDD_Clamp	VDD Zener Clamp Voltage	I(VDD) = 7 mA	24	26	28	V
Control Function Section (FB Pin)						
VFBREF	Internal Error Amplifier (EA) Reference Input		1.24	1.25	1.26	V
VFB_SLP	Short Load Protection (SLP) Threshold			0.5		V
VFB_OVP	FB Over Voltage Protection Threshold		1.48	1.56	1.64	V
TFB_short	Short Load Protection (SLP) Debounce Time	(Note 5)		42		ms
TFB_OVP	FB Over Voltage Protection Debounce Time	(Note 5)		5		TSW
VFB_dem	Demagnetization Comparator Threshold	Upper Threshold		20		mV
		Lower Threshold		0		mV
Tblank	Leading Edge Blanking Time	CC Mode (Note 5)	3.6	4	4.4	us
		CV Mode (Note 5)	1.8	2	2.2	us
Ton_max	Maximum ON time	(Note 5)		25		us
Toff_max	Maximum OFF time			3.3		ms
ICable_max	Maximum Cable Drop Compensation(CDC) Current			48		uA
TSW/Tdem	Ratio between Switching Period and Demagnetization Time in CC Mode			2		
Current Sense Input Section (CS Pin)						
TLEB	CS Input Leading Edge Blanking Time			450		ns
VCS(max)	Current limiting threshold		560	570	580	mV
VCS(min)	Current limiting threshold		215	230	245	mV

TD_OC	Over Current Detection and Control Delay			100		ns
On-Chip Thermal Shutdown						
TSD	Thermal Shutdown	(Note 5)	--	160	--	℃
TRC	Thermal Recovery	(Note 5)	--	135	--	℃
Power BJT Section (C Pin)						
IC	Maximum DC Collector Current	DP2312HTFA		0.8		A
VCE(sat)	Collector-Emitter Saturation Voltage	IC=0.2A, IB=40mA		0.3	0.6	V
HFE	DC Current Gain		15		30	
VCBO	Collector-Base Breakdown Voltage	DP2312HTFA	800			V

Note4. Stresses listed as the above "Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to maximum rating conditions for extended periods may remain possibility to affect device reliability.
Note5. Guaranteed by the Design.

CHARACTERIZATION PLOTS





OPERATION DESCRIPTION

DP2312HTFA is a high performance, multi-mode, Primary Side Regulation (PSR) power switch. The built-in high precision CV/CC control with high level protection features makes it suitable for offline small power converter applications

- **System Start-Up Operation**

Before the IC starts to work, it consumes only startup current (typically 1.1uA) which allows a large value startup resistor to be used to minimize the standby power loss. When VDD reaches turn-on voltage of 10.5V (typical), DP2312HTFA begins switching and the IC operation current is increased to be 0.26mA (typical). The hold-up capacitor continues to supply VDD before the auxiliary winding of the transformer takes control.

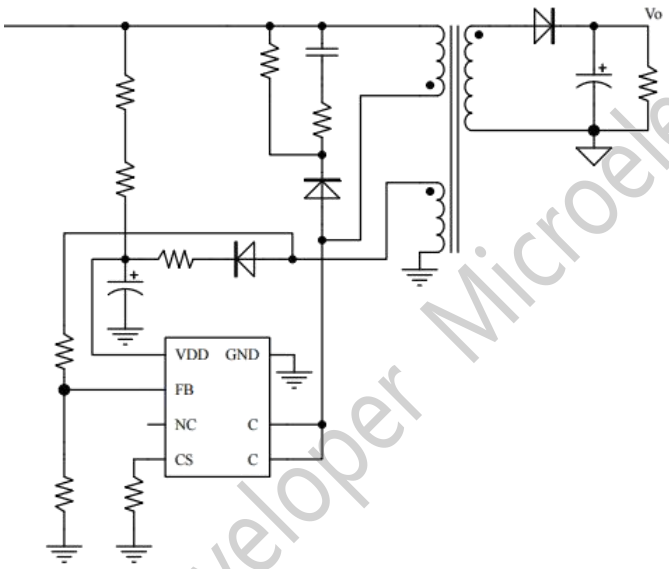


Fig 1

- **PSR CV Modulation (PSR-CVM)**

In Primary Side Regulation (PSR) control, the output voltage is sensed on the auxiliary winding during the transfer of transformer energy to the secondary. Fig.2 illustrates DP2312HTFA internal voltage sampling, the timing waveform of CV sampling signal, demagnetization signal (DEM). When the CV sampling process is over, the internal sample/hold (S&H) circuit captures the error signal and amplifies it through the internal Error Amplifier (EA). The output of EA is sent to the PSR CV Modulator (PSR-CVM) for CV regulation. The internal reference voltage for EA is trimmed to 1.25V with high accuracy.

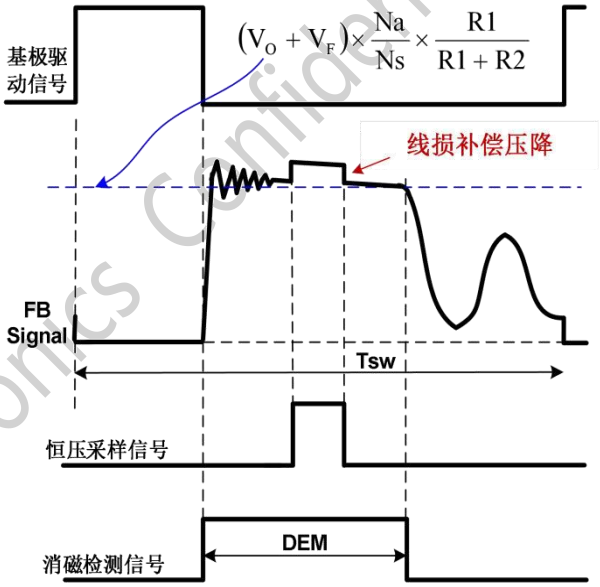


Fig 2

During the CV sampling process, DP2312HTFA internal variable current source is flowing to FB pin for Cable Drop Compensation (CDC). Thus, there is a step at FB pin in the transformer demagnetization process, as shown in Fig.2. Fig.2 also illustrates the equation for "demagnetization plateau",

$$V_{FB} = (V_O + V_F) \times \frac{Na}{Ns} \times \frac{R1}{R1+R2}$$

Where Vo and VF is the output voltage and diode forward voltage; R1 and R2 is the resistor divider connected from the auxiliary winding to FB Pin, Ns and Na is secondary winding and auxiliary winding respectively.

When heavy load condition, the Mode Selector (as

shown in "**Block Diagram**") based on EA output will switch to CC Mode automatically.

- **PSR CV Modulation (PSR-CVM)**

Timing information at the FB pin and current information at the CS pin allow accurate regulation of the secondary average current. The control law dictates that as power is increased in CV regulation and approaching CC regulation the primary peak current is at Ipp (max), as shown in Fig.3.

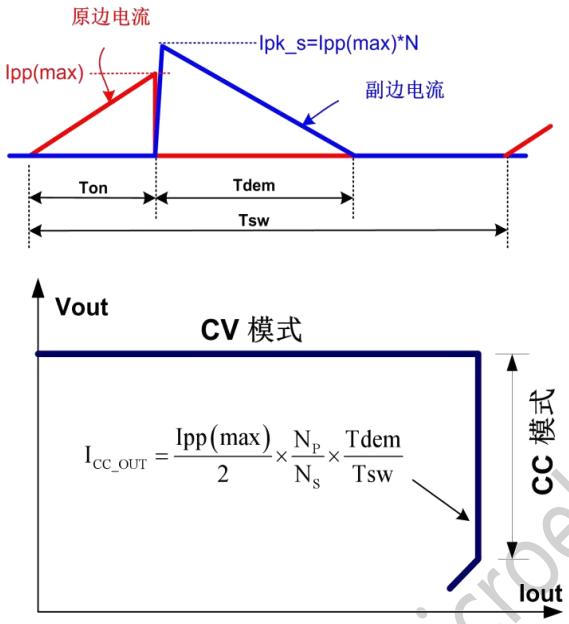


Fig 3

Referring to Fig.3 above, the primary peak current, transformer turns ratio, secondary demagnetization time (Tdem), and switching period (Tsw) determines the secondary average output current Iout. Ignoring leakage inductance effects, the equation for average output current is shown in Fig.3. When the average output current Iout reaches the regulation reference in the Primary Side Constant Current Modulator (PSR-CCM) block, the IC operates in pulse frequency modulation (PFM) mode to control the output current at any output voltage at or below the voltage regulation target as long as the auxiliary winding can keep VDD above the UVLO turn-off threshold.

In DP2312HTFA, the ratio between Tdem and Tsw in CC mode is 1/2. Therefore, the average output current can be expressed as:

$$I_{cc\_out}(mA)\cong\frac{1}{4}\times N\times\frac{570\,mV}{Rcs(\Omega)}$$

In the equation above,

N----The turn ratio of primary side winding to secondary side winding.

Rcs--- the sensing resistor connected between the power BJT emitter to GND.

- **Multi-Mode Control in CV Mode**

To meet the tight requirement of averaged system efficiency and no-load power consumption, a hybrid of frequency modulation (FM) and amplitude modulation (AM) is adopted in DP2312HTFA which is shown in the Fig 4.

Around the full load, the system operates in FM mode. When normal to light load conditions, the IC operates in FM+AM mode to achieve excellent regulation and high efficiency. When the system is near zero loading, the IC operates in FM again for standby power reduction. In this way, the no-load consumption can be less than 30mW

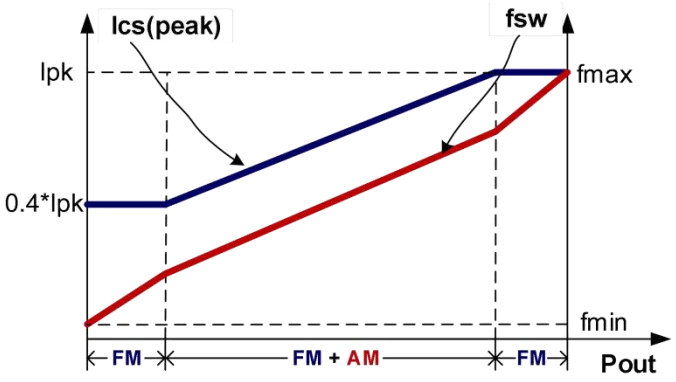


Fig 4

- **Cable Drop Compensation (CDC) in CV Mode**

In smart phone charger application, the battery is always connected to the adapter with a cable wire which can cause several percentages of voltage drop on the actual battery voltage. In DP2312HTFA, an offset voltage is generated at FB pin by an internal current source (modulated by CDC block, as shown in Fig.5) flowing into the resistor divider. The current is proportional to the switching period; thus, it is inversely proportional to the output power Pout. Therefore, the drop due the cable loss can be compensated. As the load decreases from full loading to zero loading, the offset voltage at FB pin will increase. The percentage of maximum compensation is given by:

$$\frac{\Delta V(cable)}{Vout} \approx \frac{Icable\_max \times (R1//R2)}{V_{FB\_REF}} \times 100\%$$

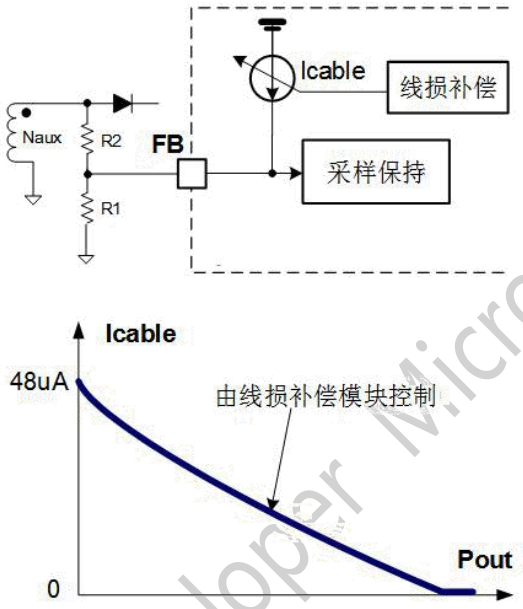


Fig 5

For example, R1=2KΩ, R2=16KΩ, The percentage of maximum compensation is given by

$$\frac{\Delta V(cable)}{Vout} \approx \frac{48u \times (16k//2k)}{1.25} \times 100\% = 6.83\%$$

- **Fast Dynamic Response**

In DP2312HTFA, the dynamic response performance is optimized to meet USB charge requirements.

- **Single Failure Protections for Power Supply**

DP2312HTFA integrates single failure protections, including FB pull-up resistor open protection, FB pull-down resistor open protection, FB pull-down resistor short protection, output rectifier diode or SR open protection, output rectifier diode or SR short protection, transformer windings short protection and Rcs open protection. This function can ensure there is no damage to IC and no over voltage of output.

- **On Chip Thermal Shutdown (OTP)**

When the IC temperature is over 160°C, the IC shuts down. Only when the IC temperature drops to 135°C, IC will restart

- **Audio Noise Free Operation**

As mentioned above, the multi-mode CV control with a hybrid of FM and AM provides frequency modulation is used in CV mode. An internal current source flowing to CS pin makes CS peak voltage modulation realized. In DP2312HTFA, the optimized combination of frequency modulation and CS peak voltage modulation algorithm can provide audio noise free operation from full loading to zero loading.

- **Dynamic BJT Base Drive**

DP2312HTFA integrates a dynamic base drive control to optimize efficiency. The BJT base drive current is dynamically controlled according to the power supply load change. The higher the output power, the higher the based current.

- **Short Load Protection (FB SLP)**

In DP2312HTFA, the output is sampled on FB pin and then compared with a threshold of UVP (0.5V typically).

In DP2312HTFA, when sensed FB voltage is below 0.5V and hold 42ms, the IC will enter into Short Load Protection (SLP) mode, in which the IC will enter into auto recovery protection mode

- **FB Over Voltage Protection (FB OVP)**

In DP2312HTFA, the output is sampled on FB pin and then compared with a threshold of OVP (1.56V typically).

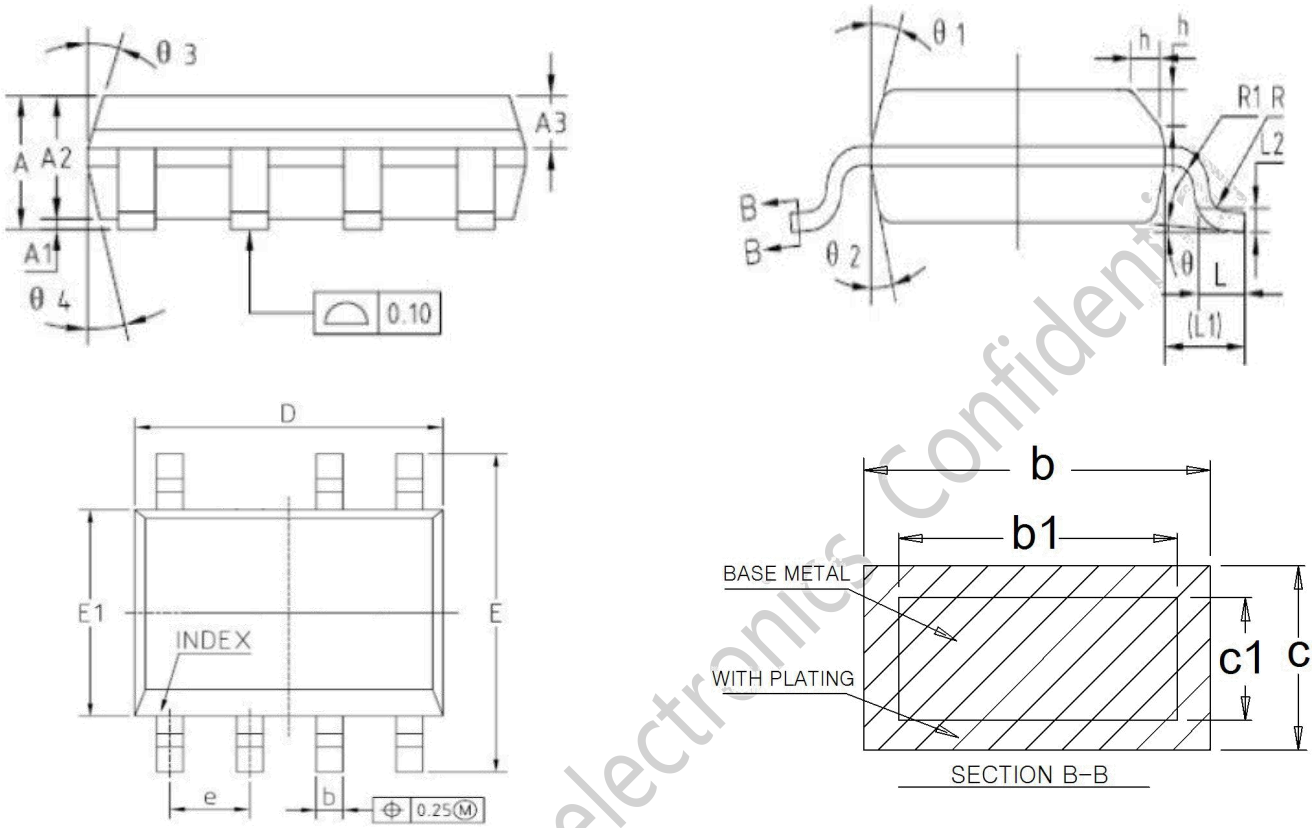
When sensed FB voltage is above 1.56V for more than 5 cycles, the IC will enter into Over Voltage Protection (OVP) mode, in which the IC will enter into auto recovery protection mode

- **VDD Over Voltage Protection (OVP) and Zener Clamp**

When VDD voltage is higher than 23V (typical), the IC will stop switching. This will cause VDD fall down to be lower than V_{DD_OFF} (typical 3.6V) and then the system will restart up again. An internal 26V (typical) zener clamp is integrated to prevent the IC from damage.

PACKAGE DIMENSION

SOP7



Symbol	Dimensions in Millimeters		
	Min	Nom	Max
A	1.45	1.55	1.65
A1	0.10	0.15	0.20
A2	1.353	1.40	1.453
A3	0.55	0.60	0.65
b	0.38	-	0.51
b1	0.37	0.42	0.47
c	0.17	-	0.25
c1	0.17	0.20	0.23
D	4.85	4.90	4.95
E	5.85	6.00	6.15
E1	3.85	3.90	3.95
e	1.245	1.27	1.295
L	0.45	0.60	0.75
L1	-	1.050REF	-
L2	-	0.250BSC	-
Θ1-Θ4	12° REF		
h	0.40REF		
R	0.15° REF		
R1	0.15° REF		

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