30V, 3A Monolithic Buck Converter with CC/CV Control

FEATURES

- 3A continuous output current capability
- 8V to 30V wide operating input range with input Over Voltage Protection
- Up to 93% efficiency
- CV Mode control (Constant voltage). Cycle-by-Cycle Current Limiting
- Output voltage accuracy: ±5%
- Fixed line drop compensation(typ 0.2V@3A)
- Fixed switching frequency is 130kHz
- Input undervoltage protection
- Output short circuit protection
- Over temperature protection
- SOP8 Package

DESCRIPTIONS

DP3122F integrates a high efficiency synchronous step-down switching regulator, which includes a high side P-MOS and a low side N-MOS to provide 3A continuous load current over 10V to 30V wide operating input voltage with 30V input over voltage protection. Conductance Peak current mode control provides fast transient responses and cycle-by-cycle current limiting. DP3122F has fixed line drop compensation. Includes a variety of protection functions:Input undervoltage, Input overvoltage protection,Output short circuit protection and Over temperature protection. A simple Power system with few external components is possible with DP3122F.

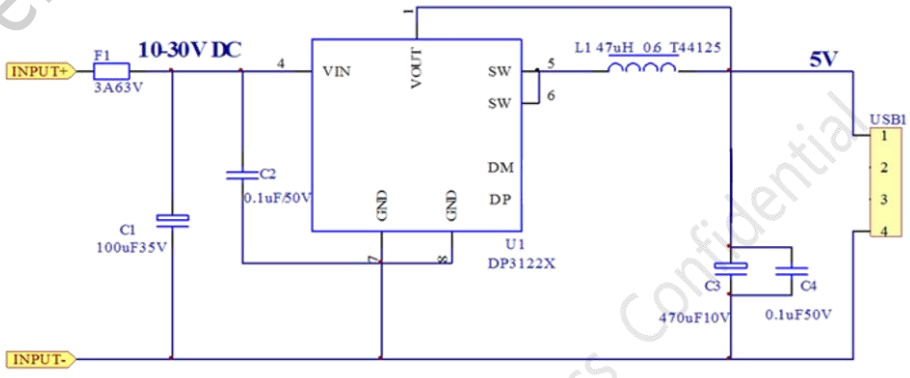
APPLICATIONS

- USB car charger
- Portable charging device
- Quick charging A+C charger
- General purpose DC-DC conversion

ORDERING INFORMATION

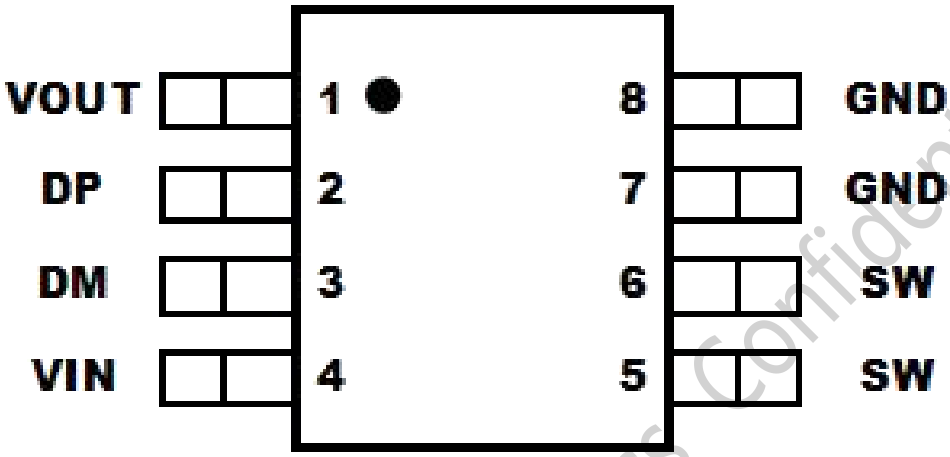
Part Number	Description
DP3122F	SOP8, Pb free in T&R, 4000 Pcs/Reel

TYPICAL APPLICATION CIRCUIT



PRODUCT DESCRIPTION

➢ Pin Configuration



➢ Pin Description

Pin Number	Pin Name	Description
1	VOUT	Output voltage detection pin
2	DP	USB data transfer DP pin，No Connect
3	DM	USB data transfer DM pin, No Connect
4	VIN	Power Input PIN. Vin supplies the power to the IC. Supply Vin with a 8V to 30V power source. Bypass Vin to GND with a large capacitor and at least another 0.1uF ceramic capacitor to eliminate noise on the input to the IC. Put the capacitors close to Vin and **GND** pins.
5	SW	Power Switching pin. Connect this pin to the switching node of inductor.
6	SW	Power Switching pin. Connect this pin to the switching node of inductor.
7	GND	GROUND
8	GND	GROUND

➢ Marking Information

DP3122F for product name:

XXXXXX The first X represents the last year,2020 is 0;The second X represents the month,inA-L 12 letters;The third and fourth X on behalf of the date,01-31said;The last two X represents the wafer batch code.

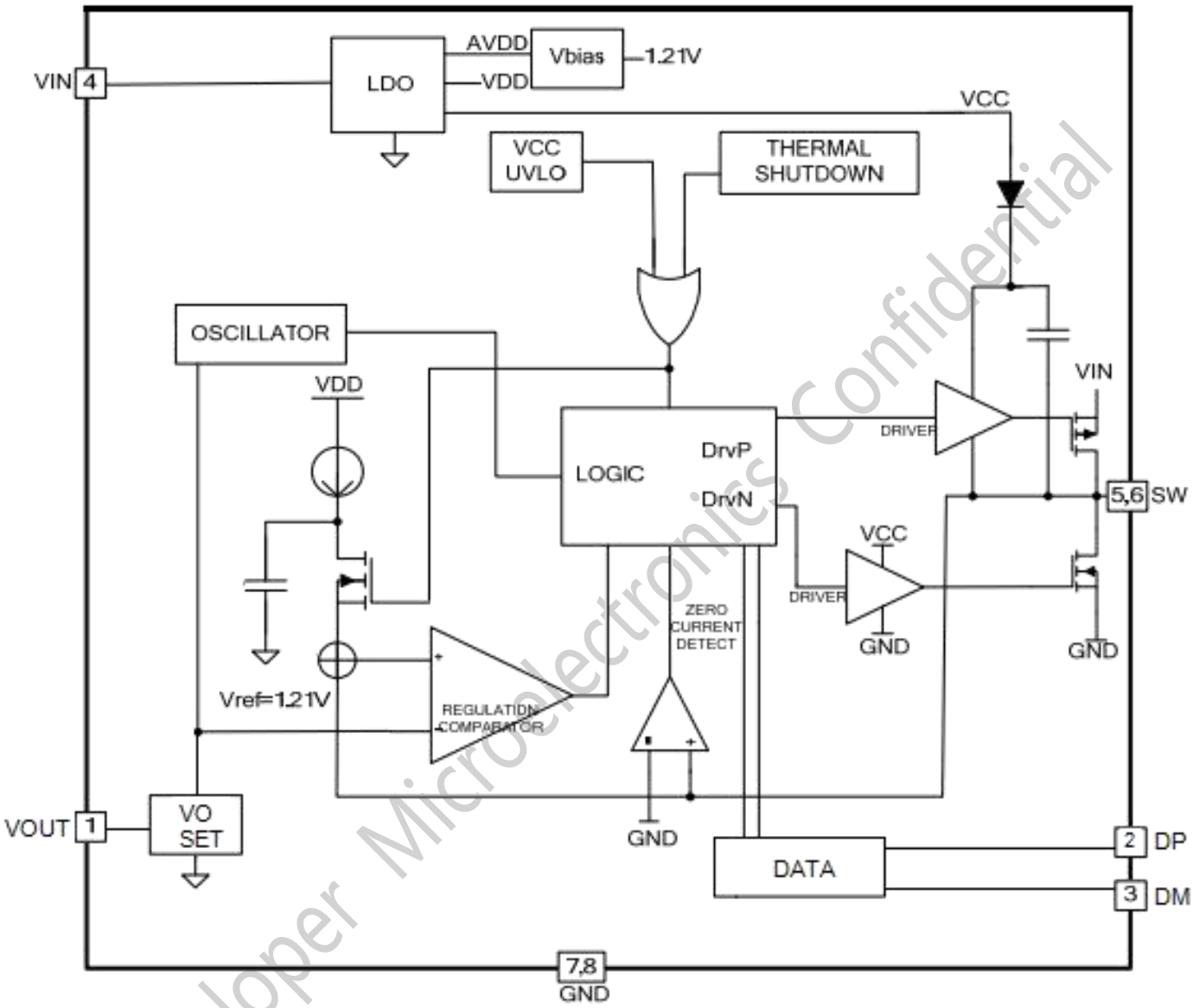
➢ Absolute Maximum Ratings

PARAMETER	PROJECT	MIN	MAX	Unit
Input Voltages	V_{IN} to GND	-0.3	36	V
	V_{DP} to GND	-0.3	3	V
	V_{DM} to GND	-0.3	3	V
	V_{OUT} to GND	-0.3	6	V
	V_{SW} to GND	-0.3	VIN+1	V

➢ Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	Unit
T_{ST}	Storage Temperature Range	-65	150	°C
T_J	Junction Temperature	-	150	°C
T_L	Lead Temperature	-	260	°C

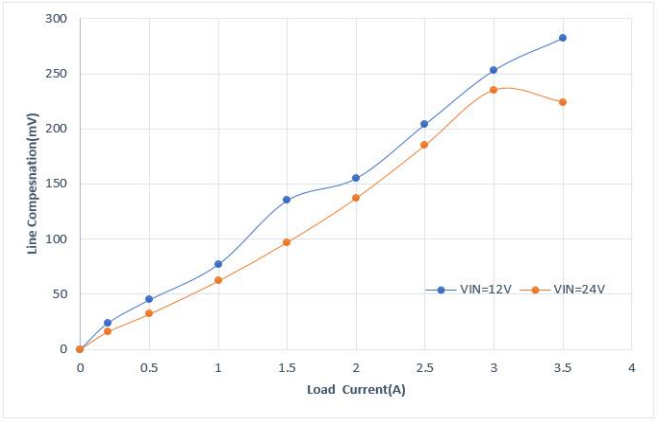
BLOCK DIAGRAM



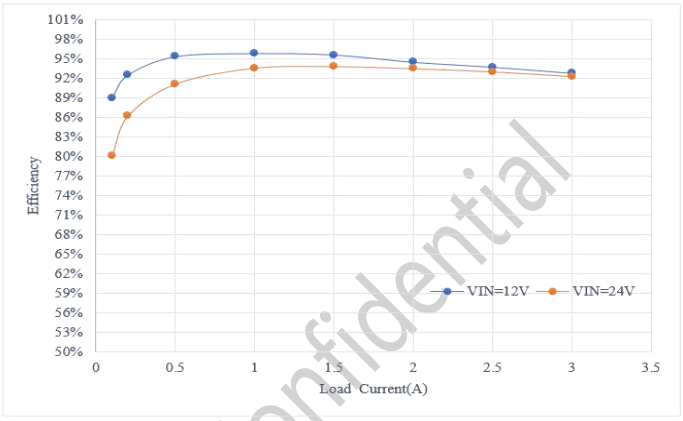
ELECTRICAL CHARACTERISTICS (Typical at Vin = 12V, TJ=25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Voltage	VIN		8		30	V
No-load current	ICC	ILOAD=0A		0.2		mA
Input UVLO	Vuvlo			7.5		V
Input UVLO hysteresis voltage	ΔVuvlo			0.6		V
Voltage of VOUT	VOUT	ILOAD=0A	4.80	5.05	5.25	V
operating frequency range	FOSC		100	130	160	KHZ
Max duty cycle	DC				100	%
R_{DSON} of P-MOS	RPFET	DP3122F (5V3A)		54		mΩ
R_{DSON} of N-MOS	RNFET	DP3122F (5V3A)		27		mΩ
Output Voltage Protection	VOVP-OUT			6		V
Output Short Protection	VSHORT			2.4		V
INPUT Short Current	IVIN-SHORT			5		mA
Over-Temperature Protection	TSD			150		℃
Over-Temperature Protection hysteresis	△TSD			30		℃

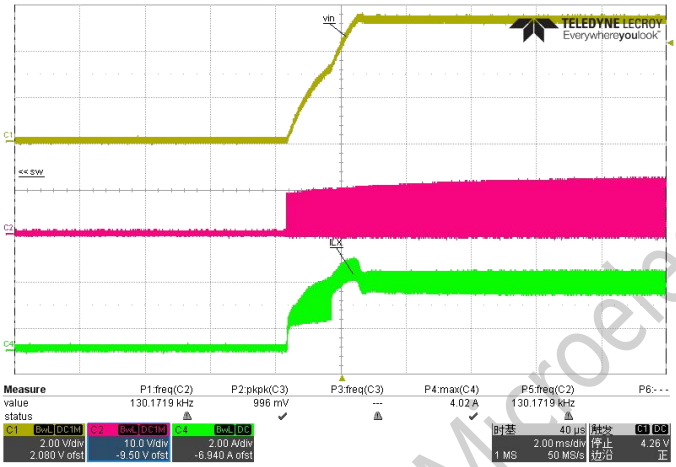
TYPICAL CHARACTERISTICS(Typical at Vin = 12V, Vout=5V TJ=25°C, unless otherwise noted.)



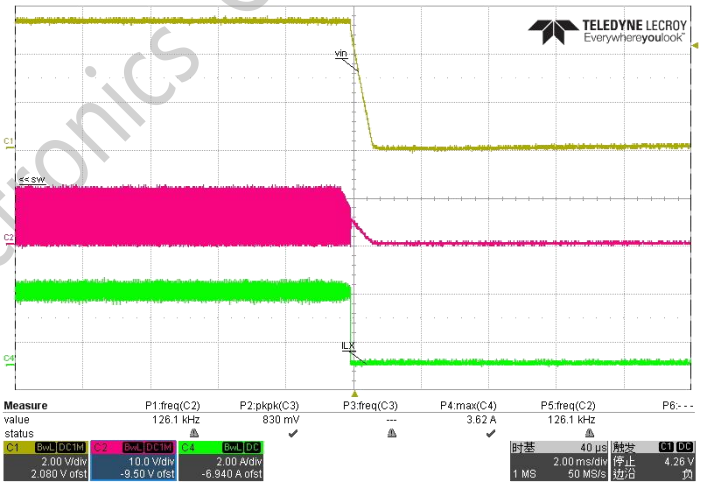
LINE COMPENSATION



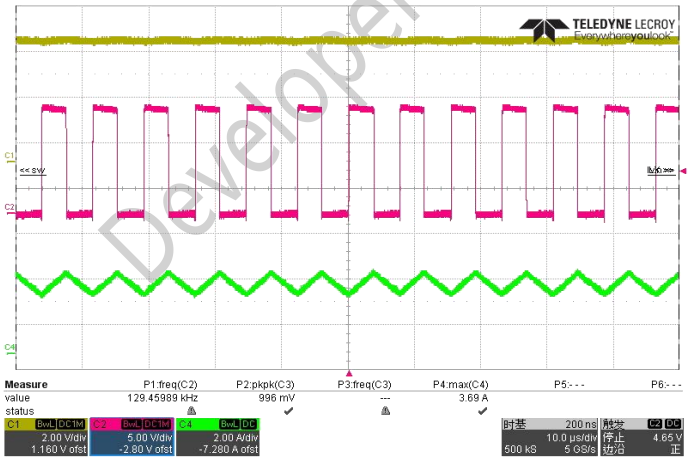
EFFICIENCY



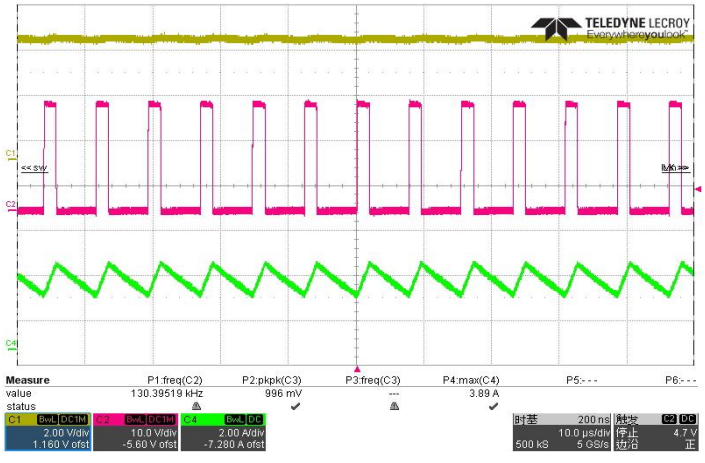
Startup waveform



Stutdown waveform



VIN:12V Steady state waveform



VIN:24V Steady state waveform

APPLICATION INFORMATION

DP3122F adopts the peak current control mode with fixed frequency, The output voltage is detected by VOUT pin. The lower bias current of FB is regulated by detecting the Ipeak of the inductor and VOUT , And the internal P-MOS and N-MOS switches are controlled and driven by an internal oscillator , achieve constant current and stable output voltage. When P-MOS is ON, N-MOS is OFF.

- **Thermal Shutdown**

The internal thermal-shutdown circuitry forces the device to stop switching if the junction temperature exceeds 150°C typically.

- **Inductance peak current limiting**

DP3122F Limit the P-MOS peak current to limit input power, DP3122F detect the peak current of P-MOS at toff of every cycle, if higher than the set limit DP3122F will shut down the P-MOS. When the temperature rise up, the RDSON of P-MOS will become larger

- **Oscillation frequency**

The oscillation frequency of DP3122F is fixed at 130KHZ

- **Output Shutdown voltage**

DP3122F will shutdown the output if the output voltage is lower than about 2V when the output load is too heavy

- **Line drop compensation**

If USB cable is too long or resistance value is high, the voltage of charging device end will be dropped a lot. If the voltage across the load input terminals is too low, it will affect charging time. So recommend to adjust the output voltage of charger to compensate this voltage drop. The line drop compensation value of DP3122F is fixed at 0.2V@3A.

- **Inductor selection**

An inductor is required to supply constant current to the load while being driven by the switched input voltage. The common value of the inductance is between 4.7uH to 47uH. A larger value inductor will result in less current ripple and lower output voltage ripple. However, the larger value inductor will have larger physical size, higher DC resistance, and/or lower saturation current. A good rule to calculate the inductance is to allow the peak-to-peak ripple current in the inductor to be approximately 25% of the maximum load current. At the same time, it is needed to make sure that the peak inductor current is below the inductor saturation current.
The inductance value can be calculated by:

$$L=\frac{V_{OUT}}{f_s\times\Delta I_L}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

Where VOUT is the output voltage, VIN is the input voltage, fs is the switching frequency, and ΔL is the peak-to-peak inductor ripple current.
The choice of which style inductor to use mainly depends on the price vs. size requirements and any EMI constraints.

- **Input capacitors selection**

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the converter. It is recommend to use low ESR capacitors to optimize the performance. Ceramic capacitor is preferred, but tantalum or low-ESR electrolytic capacitors may also meet the requirements. It is better to choose X5R or X7R dielectrics when using ceramic capacitors.
Since the input capacitor (CIN) absorbs the input switching current, a good ripple current rating is required for the capacitor. The RMS current in the input capacitor can be estimated by:

$$I_{CIN}=I_{load}\times\sqrt{\frac{V_{OUT}}{V_{IN}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)}$$

The worst-case condition occurs at VIN = 2×VOUT, where:

$$I_{CIN}=\frac{I_{load}}{2}$$

For simplification, choose the input capacitor whose RMS current rating is greater than half of the maximum load current. When electrolytic or tantalum capacitors are used, a small, high quality ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible. When ceramic capacitors are used, make sure that they have enough capacitance to maintain voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN}=\frac{I_{load}}{f_s\times C_{IN}}\times\frac{V_{OUT}}{V_{IN}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

CIN is the input capacitance.

- **Output capacitors selection**

The output capacitor (COUT) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended.
Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT}=\frac{V_{OUT}}{f_s\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times\left(R_{ESR}+\frac{1}{8\times f_s\times C_{OUT}}\right)$$

Where L is the inductor value, RESR is the equivalent series resistance (ESR) value of the output capacitor and COUT is the output capacitance value. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly determined by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT}=\frac{V_{OUT}}{8\times f_s^{2}\times L\times C_{OUT}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT}=\frac{V_{OUT}}{f_s\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The DP3122F can be optimized for a wide range of capacitance and ESR values.

- **PCB Layout**

PCB layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion efficiency, thermal performance, and minimized EMI.

1. Vout sense path should stay away from noisy nodes, such as SW signals and preferably through a layer on the other side of shielding layer.

2. The input bypass capacitor C1 and C2 must be placed as close as possible to the VIN pin and ground. Grounding for both the input and output capacitors should consist of localized top side planes that connect to the GND pin and PAD. It is a good practice to place a ceramic cap near the VIN pin to reduce the high frequency injection current.

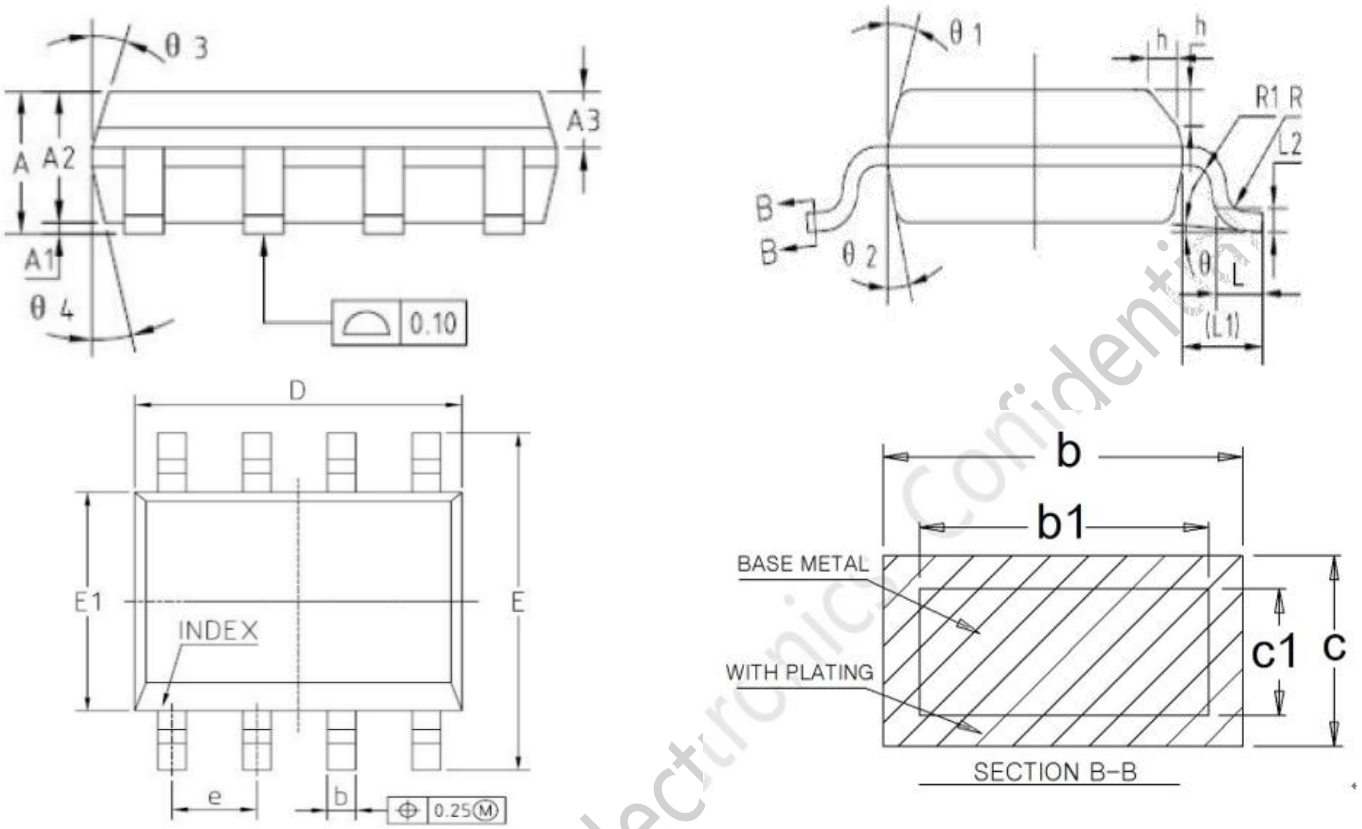
3. The inductor L should be placed close to the SW pin to reduce magnetic and electrostatic noise.

4. The output capacitor, C3 should be placed close to the junction of L. The L, and COUT trace should be as short as possible to reduce conducted and radiated noise and increase overall efficiency.

5. The ground connection for C1, C2 and C3, C4 should be as small as possible and connect to system ground plane at only one spot (preferably at the C3 ground point) to minimize injecting noise into system ground plane. Large GND Copper Pour near IC is recommended to minimize the heat of DP3122F.

PACKAGE DIMENSION

SOP8



Symbol	Dimensions in Millimeters		
	Min	Nom	Max
A	1.45	1.55	1.65
A1	0.10	0.15	0.20
A2	1.353	1.40	1.453
A3	0.55	0.60	0.65
b	0.38	-	0.51
b1	0.37	0.42	0.47
c	0.17	-	0.25
c1	0.17	0.20	0.23
D	4.85	4.90	4.95
E	5.85	6.00	6.15
E1	3.85	3.90	3.95
e	1.245	1.27	1.295
L	0.45	0.60	0.75
L1	-	1.050REF	-
L2	-	0.250BSC	-
Θ1-Θ4	12° REF		
h	0.40REF		
R	0.15° REF		
R1	0.15° REF		

REVISION HISTORY

Editions	Revised Date	Redaction person	Revision content
REV1.0	2024/4/8	PXB	First release

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